David M. Barkan (#160825/barkan@fr.com)
FISH & RICHARDSON P.C.
500 Arguello St., Suite 500
Redwood City, CA 94063
Telephone: (650) 839-5070
Facsimile: (650) 839-5071

Barry K. Shelton (#199307; shelton@fr.com)
FISH & RICHARDSON P.C.
111 Congress Avenue, Suite 810
Austin, Texas 78701
Telephone: (512) 472-5070
Facsimile: (512) 320-8935

Attorneys for Plaintiff
MARVELL SEMICONDUCTOR, INC.

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

C07 05626 WDB

CJ WDB

MARVELL SEMICONDUCTOR, INC., a California corporation, Plaintiff, v. WI-LAN, INC., a Canadian corporation, Defendant	CASE NO. **COMPLAINT FOR DECLARATORY RELIEF;** **DEMAND FOR JURY TRIAL**

ORIGINAL

COMPLAINT AND JURY DEMAND

Plaintiff Marvell Semiconductor, Inc. ("Marvell"), for its complaint against defendant Wi-LAN, Inc. ("Wi-LAN") alleges:

I. THE PARTIES

1. Marvell is a corporation organized under the laws of the state of California. Marvell's principal place of business is 5488 Marvell Lane, Santa Clara, California 95054.

2. Upon information and belief, Wi-LAN is a corporation organized under the Business Corporations Act (Alberta), in Canada. Upon information and belief, Wi-LAN's principal place of business is 11 Holland Avenue, Suite 608, Ottawa, Ontario, K1Y 4S1.

II. JURISDICTION AND VENUE

3. This action arises under the Federal Declaratory Judgments Act, 28 U.S.C. §§ 2201 and 2202, and the patent laws of the United States, 35 U.S.C. § 1 *et seq*. An actual, substantial and continuing justiciable controversy exists between Plaintiff and Wi-LAN that requires a declaration of rights by this Court.

4. The Court has subject mater jurisdiction pursuant to 28 U.S.C. §§ 1331, 1337, and 1338.

5. The Court has personal jurisdiction over Wi-LAN by virtue of Wi-LAN's purposeful and repeated contacts in this district, including, *inter alia*, the dispatching of agents in this district in an attempt to license U.S. Reissued Patent No. RE37,802 ("the '802 patent"), U.S. Patent No. 6,192,068 ("the '068 patent"), and U.S. Patent No. 6,320,897 ("the '897 patent") to Plaintiff and to other companies in this district; and Wi-LAN's threats to enforce the '802, '068, and '897 patents against companies with principal places in this district.

6. Upon information and belief, Wi-LAN has engaged in a campaign to license the '802, '068, and '897 patents to a number of companies located in northern California, including Marvell and others. On numerous occasions, Wi-LAN has participated in face-to-face meetings with a number of said companies in northern California and demanded that they take a license to the '802, '068, and '897 patents.

7. Venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391 and 1400.

III. FACTUAL BACKGROUND

8. U.S. Reissued Patent No. RE37,802, entitled "Multicode Direct Sequence Spread Spectrum," was filed on September 10, 1998 and reissued on July 23, 2002. The '802 was reissued from U.S. Patent No. 5,555,268, which was filed on January 24, 1994 and issued on September 10, 1996. The '802 names as inventors Michel Fattouche and Hatim Zaghloul. The '802 patent is attached as Exhibit A.

9. U.S. Patent No. 6,192,068, entitled "Multicode Spread Spectrum Communications System," was filed on October 3, 1996 and issued on February 20, 2001. The '068 names as inventors Michel Fattouche, Hatim Zaghloul, Paul Milligan, and David Snell. The '068 patent is attached as Exhibit B.

10. U.S. Patent No. 6,320,897, entitled "Multicode Spread Spectrum Communications System," was filed on September 3, 1999 and issued on November 20, 2001. The '897 patent was a continuation of the application that issued as the '068 patent. The '897 names as inventors Michel Fattouche, Hatim Zaghloul, Paul Milligan, and David Snell. The '897 patent is attached as Exhibit C.

A. Wi-LAN Demands that Marvell License the '802, '068, and '897 Patents

11. On or about December 15, 2006, Mr. William Middleton, Vice President, General Counsel & Secretary of Wi-LAN, sent an email to Mr. Matthew Gloss at Marvell identifying the '802, '068, and '897 patents and asserting that the patents covered Marvell's PxA90x communications processor integrated circuit family.

12. On or about December 21, 2006, Mr. Middleton reiterated in a letter to Mr. Gloss Wi-LAN's assertion that the manufacture and sale of the identified Marvell products infringed the '802, '068, and '897 patents and that the products "require a license" to the these patents.

13. On or about December 29, 2006, Mr. Michael Molano of Mayer, Brown, Rowe & Maw LLP, outside counsel to Marvell, responded by letter to Mr. Middleton's communications, and requested that Wi-LAN provide Marvell with infringement claim charts and the file histories for the '802, '068, and '897 patents. Wi-LAN never responded to Mr. Molano's letter.

14. On or about July 18, 2007, Mr. Barry K. Shelton of Fish & Richardson P.C., outside counsel to Marvell, sent an email to Mr. Middleton reiterating Marvell's request that Wi-LAN provide infringement claim charts and the file histories for the '802, '068, and '897 patents, or, alternatively, that Wi-LAN confirm it no longer asserted that Marvell infringed any of the previously identified patents.

15. On or about August 8, 2007, Mr. Middleton replied via email to Mr. Shelton and stated that Wi-LAN would provide the requested infringement claim charts under separate cover. As of the filing of this complaint, no claim charts or further response had been received from Wi-LAN.

16. On October 31, 2007, Wi-LAN filed two complaints in the Eastern District of Texas, Marshall Division (Civil Action Nos. 2-07CV-473 and 2-07CV-474, collectively "the Texas Actions"), each accusing Plaintiff Marvell of infringing U.S. Patent No. 5,282,222 and the '802 patent "by making, using, offering for sale, importing, and/or selling integrated circuits and/or circuit boards used and/or designed for use" in accused products manufactured by other defendants.

17. On November 1, 2007, Wi-LAN held a public conference call regarding the Texas Actions, during which Wi-LAN CEO Jim Skippen confirmed that the Texas Actions were the "two initial waves" of litigation.

18. Based on Wi-LAN's assertions of patent infringement by Marvell, an actual, substantial and continuing justiciable controversy exists between Plaintiff Marvell and Wi-LAN that requires a declaration of rights by this Court.

FIRST COUNT

DECLARATORY JUDGMENT – NONINFRINGEMENT OF THE '802 PATENT

19. Plaintiff incorporates by reference the allegations in paragraphs 1 through 18, inclusive.

20. This is an action for declaratory judgment of noninfringement of any and all valid claims of the '802 patent.

21. Plaintiff has an objectively reasonable apprehension that Wi-LAN will bring a patent infringement action on the '802 patent against Plaintiff and/or Plaintiff's respective customers.

22. Wi-LAN has alleged that it "holds all rights and interest in the '802 patent."

23. Wi-LAN has alleged and continues to allege that Plaintiff has directly infringed, and induced and/or contributed to the infringement of the '802 patent.

24. Plaintiff denies Wi-LAN's allegation with respect to infringement by Plaintiff or Plaintiff's respective customers. Neither Plaintiff nor its respective customers directly infringe, either literally or under the doctrine of equivalents, or induce or contribute to the infringement of, any valid claim of the '802 patent.

25. Accordingly, there exists an actual, justiciable controversy between Plaintiff and Wi-LAN relating to whether Plaintiff or Plaintiff's respective customers infringe the claims of the '802 patent.

26. Plaintiff desires and requests a judicial determination and declaration of the respective rights and duties of the parties based on the disputes recited in this complaint.

SECOND COUNT

DECLARATORY JUDGMENT – NONINFRINGEMENT OF THE '068 PATENT

27. Plaintiff incorporates by reference the allegations in paragraphs 1 through 26, inclusive.

28. This is an action for declaratory judgment of noninfringement of any and all valid claims of the '068 patent.

29. Plaintiff has an objectively reasonable apprehension that Wi-LAN will bring a patent infringement action on the '068 patent against Plaintiff and/or Plaintiff's respective customers.

30. Wi-LAN has alleged that it "holds all rights and interest in the '068 patent."

31. Wi-LAN has alleged and continues to allege that Plaintiff has directly infringed, and induced and/or contributed to the infringement of the '068 patent.

32. Plaintiff denies Wi-LAN's allegation with respect to infringement by Plaintiff or Plaintiff's respective customers. Neither Plaintiff nor its respective customers directly infringe, either literally or under the doctrine of equivalents, or induce or contribute to the infringement of, any valid claim of the '068 patent.

33. Accordingly, there exists an actual, justiciable controversy between Plaintiff and Wi-LAN relating to whether Plaintiff or its respective customers infringe the claims of the '068 patent.

34. Plaintiff desires and requests a judicial determination and declaration of the respective rights and duties of the parties based on the disputes recited in this complaint.

THIRD COUNT

DECLARATORY JUDGMENT – NONINFRINGEMENT OF THE '897 PATENT

35. Plaintiff incorporates by reference the allegations in paragraphs 1 through 34, inclusive.

36. This is an action for declaratory judgment of noninfringement of any and all valid claims of the '897 patent.

37. Plaintiff has an objectively reasonable apprehension that Wi-LAN will bring a patent infringement action on the '897 patent against Plaintiff and/or Plaintiff's respective customers.

38. Wi-LAN has alleged that it "holds all rights and interest in the '897 patent."

39. Wi-LAN has alleged and continues to allege that Plaintiff has directly infringed, and induced and/or contributed to the infringement of the '897 patent.

40. Plaintiff denies Wi-LAN's allegation with respect to infringement by it or its respective customers. Neither Plaintiff nor its respective customers directly infringe, either literally or under the doctrine of equivalents, or induce or contribute to the infringement of, any valid claim of the '897 patent.

41. Accordingly, there exists an actual, justiciable controversy between Plaintiff and Wi-LAN relating to whether Plaintiff or its respective customers infringe the claims of the '897 patent.

42. Plaintiff desires and requests a judicial determination and declaration of the respective rights and duties of the parties based on the disputes recited in this complaint.

FOURTH COUNT

DECLARATORY JUDGMENT – INVALIDITY OF THE '802 PATENT

43. Plaintiff incorporates by reference the allegations in paragraphs 1 through 42, inclusive.

44. This is an action for declaratory judgment of invalidity of any and all claims of the '802 patent.

45. Plaintiff has an objectively reasonable apprehension that Wi-LAN will bring a patent infringement action on the '802 patent against Plaintiff and/or Plaintiff's customers.

46. The claims of the '802 patent are invalid because they fail to comply with the conditions and requirements for patentability set forth in 35 U.S.C. § 1 et seq., including but not limited to 35 U.S.C. §§ 101, 102, 103, 112, 115, 116, 118, 132, and 256.

47. Accordingly, there exists an actual, justiciable controversy between Plaintiff and Wi-LAN relating to whether the claims of the '802 patent are invalid.

48. Plaintiff desires and requests a judicial determination and declaration of the respective rights and duties of the parties based on the disputes recited in this complaint.

FIFTH COUNT

DECLARATORY JUDGMENT – INVALIDITY OF THE '068 PATENT

49. Plaintiff incorporates by reference the allegations in paragraphs 1 through 48, inclusive.

50. This is an action for declaratory judgment of invalidity of any and all claims of the '068 patent.

51. Plaintiff has an objectively reasonable apprehension that Wi-LAN will bring a patent infringement action on the '068 patent against Plaintiff and/or Plaintiff's customers.

52. The claims of the '068 patent are invalid because they fail to comply with the conditions and requirements for patentability set forth in 35 U.S.C. § 1 et seq., including but not limited to 35 U.S.C. §§ 101, 102, 103, 112, 115, 116, 118, 132, and 256.

53. Accordingly, there exists an actual, justiciable controversy between Plaintiff and Wi-LAN relating to whether the claims of the '068 patent are invalid.

54. Plaintiff desires and requests a judicial determination and declaration of the respective rights and duties of the parties based on the disputes recited in this complaint.

SIXTH COUNT

DECLARATORY JUDGMENT – INVALIDITY OF THE '897 PATENT

55. Plaintiff incorporates by reference the allegations in paragraphs 1 through 54, inclusive.

56. This is an action for declaratory judgment of invalidity of any and all claims of the '897 patent.

57. Plaintiff has an objectively reasonable apprehension that Wi-LAN will bring a patent infringement action on the '897 patent against Plaintiff and/or Plaintiff's customers.

58. The claims of the '897 patent are invalid because they fail to comply with the conditions and requirements for patentability set forth in 35 U.S.C. § 1 et seq., including but not limited to 35 U.S.C. §§ 101, 102, 103, 112, 115, 116, 118, 132, and 256.

59. Accordingly, there exists an actual, justiciable controversy between Plaintiff and Wi-LAN relating to whether the claims of the '897 patent are invalid.

60. Plaintiff desires and requests a judicial determination and declaration of the respective rights and duties of the parties based on the disputes recited in this complaint.

SEVENTH COUNT

DECLARATORY JUDGMENT – PATENT MISUSE ('802 PATENT)

61. Plaintiff incorporates by reference the allegations in paragraphs 1 through 60, inclusive.

62. The '802 patent is unenforceable for patent misuse, due to Wi-LAN's continuing unlawful attempts to enforce the '802 patent as alleged in this complaint.

63. On information and belief, despite Wi-LAN's knowledge and awareness that the '802 patent is invalid and unenforceable, as alleged herein, Wi-LAN has attempted and continues

to attempt to improperly obtain the economic advantage of injunctive relief and/or monetary damages against Plaintiff and its respective customers.

64. Accordingly, there exists an actual, justiciable controversy between Plaintiff and Wi-LAN concerning whether the claims of the '802 patent are unenforceable due to patent misuse.

65. Plaintiff desires and requests a judicial determination and declaration of the respective rights and duties of the parties based on the disputes recited in this complaint.

EIGHTH COUNT

DECLARATORY JUDGMENT – PATENT MISUSE ('068 PATENT)

66. Plaintiff incorporates by reference the allegations in paragraphs 1 through 65, inclusive.

67. The '068 patent is unenforceable for patent misuse, due to Wi-LAN's continuing unlawful attempts to enforce the '068 patent as alleged in this complaint.

68. On information and belief, despite Wi-LAN's knowledge and awareness that the '068 patent is invalid and unenforceable, as alleged herein, Wi-LAN has attempted and continues to attempt to improperly obtain the economic advantage of injunctive relief and/or monetary damages against Plaintiff and its respective customers.

69. Accordingly, there exists an actual, justiciable controversy between Plaintiff and Wi-LAN concerning whether the claims of the '068 patent are unenforceable due to patent misuse.

70. Plaintiff desires and requests a judicial determination and declaration of the respective rights and duties of the parties based on the disputes recited in this complaint.

NINTH COUNT

DECLARATORY JUDGMENT – PATENT MISUSE ('897 PATENT)

71. Plaintiff incorporates by reference the allegations in paragraphs 1 through 70, inclusive.

72. The '897 patent is unenforceable for patent misuse, due to Wi-LAN's continuing unlawful attempts to enforce the '897 patent as alleged in this complaint.

73. On information and belief, despite Wi-LAN's knowledge and awareness that the '897 patent is invalid and unenforceable, as alleged herein, Wi-LAN has attempted and continues

to attempt to improperly obtain the economic advantage of injunctive relief and/or monetary damages against Plaintiff and its respective customers.

74. Accordingly, there exists an actual, justiciable controversy between Plaintiff and Wi-LAN concerning whether the claims of the '897 patent are unenforceable due to patent misuse.

75. Plaintiff desires and requests a judicial determination and declaration of the respective rights and duties of the parties based on the disputes recited in this complaint.

PRAYER FOR RELIEF

A. A judgment declaring that the Plaintiff has not infringed and does not infringe in any manner any valid claim of the '802 patent;

B. A judgment declaring that the Plaintiff has not infringed and does not infringe in any manner any valid claim of the '068 patent;

C. A judgment declaring that the Plaintiff has not infringed and does not infringe in any manner any valid claim of the '897 patent;

D. A judgment declaring that each claim of the '802 patent is invalid;

E. A judgment declaring that each claim of the '068 patent is invalid;

F. A judgment declaring that each claim of the '897 patent is invalid;

G. A judgment declaring that the '802 patent is unenforceable and therefore without any force or effect against Plaintiff, its respective officers, agents, employees and customers;

H. A judgment declaring that the '068 patent is unenforceable and therefore without any force or effect against Plaintiff, its respective officers, agents, employees and customers;

I. A judgment declaring that the '897 patent is unenforceable and therefore without any force or effect against Plaintiff, its respective officers, agents, employees and customers;

J. A judgment determining this to be an "exceptional" case within the meaning of 35 U.S.C. § 285, entitling Plaintiff to an award of its reasonable attorneys' fees, expenses, and costs in this action; and

K. For such other and further relief, in law or in equity, as this Court deems just.

JURY TRIAL DEMAND

Plaintiff demands a trial by jury as to all issues and causes of action so triable herein, pursuant to Federal Rule of Civil Procedure 38.

Dated: November 5, 2007

FISH & RICHARDSON P.C.

By: David M. Barkan
David M. Barkan

Attorneys for Plaintiff
MARVELL SEMICONDUCTOR, INC.

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EXHIBIT A

US00RE37802E

(19) **United States**
(12) **Reissued Patent**
Fattouche et al.

(10) **Patent Number: US RE37,802 E**
(45) **Date of Reissued Patent: Jul. 23, 2002**

(54) **MULTICODE DIRECT SEQUENCE SPREAD SPECTRUM**

(75) Inventors: **Michel T. Fattouche**; **Hatim Zaghloul**, both of Calgary (CA)

(73) Assignee: **Wi-LAN Inc.**, Calgary (CA)

(21) Appl. No.: **09/151,604**

(22) Filed: **Sep. 10, 1998**

Related U.S. Patent Documents

Reissue of:
(64) Patent No.: **5,555,268**
Issued: **Sep. 10, 1996**
Appl. No.: **08/186,784**
Filed: **Jan. 24, 1994**

(51) **Int. Cl.**[7] **H04B 1/707**; H04B 1/69
(52) **U.S. Cl.** **375/141**; 370/209; 375/146; 375/147; 380/34
(58) **Field of Search** 375/200, 201, 375/202, 203, 204, 206, 207, 208, 209, 210, 130–153, 271, 279, 280, 322, 329, 332; 380/34, 46; 370/203, 204, 205, 206, 207, 208, 209, 210, 211; 364/717.01, 717.02, 717.03, 717.04, 717.05, 717.06, 717.07; 331/78; 714/746, 752, 778, 781, 782

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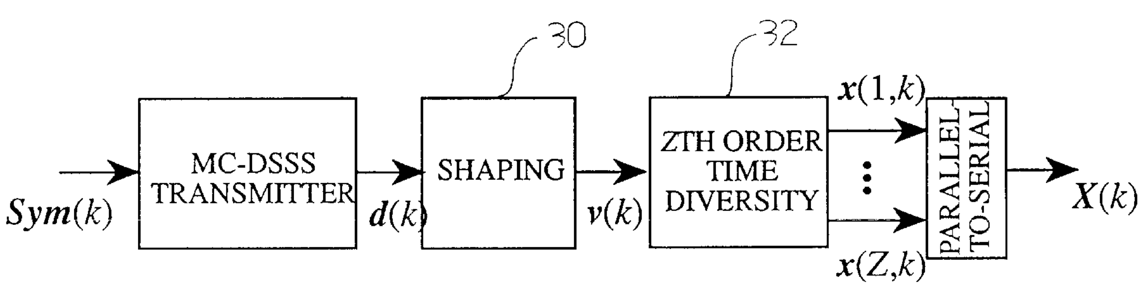
Primary Examiner—Bernarr E. Gregory
(74) *Attorney, Agent, or Firm*—Christensen O'Connor Johnson Kindness PLLC

(57) **ABSTRACT**

In this patent, we present MultiCode Direct Sequence Spread Spectrum (MC-DSSS) which is a modulation scheme that assigns up to N DSSS codes to an individual user where N is the number of chips per DSSS code. When viewed as DSSS, MC-DSSS requires up to N correlators (or equivalently up to N Matched Filters) at the receiver with a complexity of the order of N^2 operations. In addition, a non ideal communication channel can cause InterCode Interference (ICI), i.e., interference between the N DSSS codes. In this patent, we introduce new DSSS codes, which we refer to as the "MC" codes. Such codes allow the information in a MC-DSSS signal to be decoded in a sequence of low complexity parallel operations which reduce the ICI. In addition to low complexity decoding and reduced ICI. MC-DSSS using the MC codes has the following advantages: (1) it does not require the stringent synchronization DSSS requires, (2) it does not require the stringent carrier recovery DSSS requires and (3) it is spectrally efficient.

40 Claims, 20 Drawing Sheets



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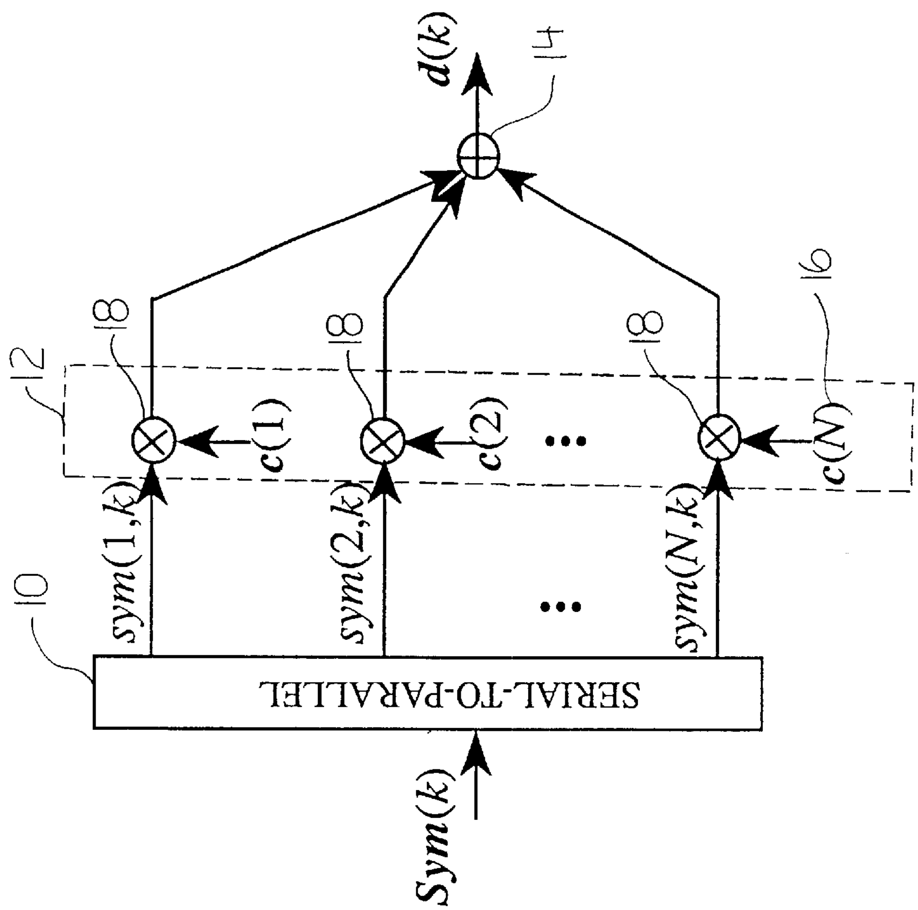

d(k)
14
18
18
18
12
16
c(1)
c(2)
c(N)
sym(1,k)
sym(2,k)
sym(N,k)
10
SERIAL-TO-PARALLEL
Sym(k)

FIGURE 1

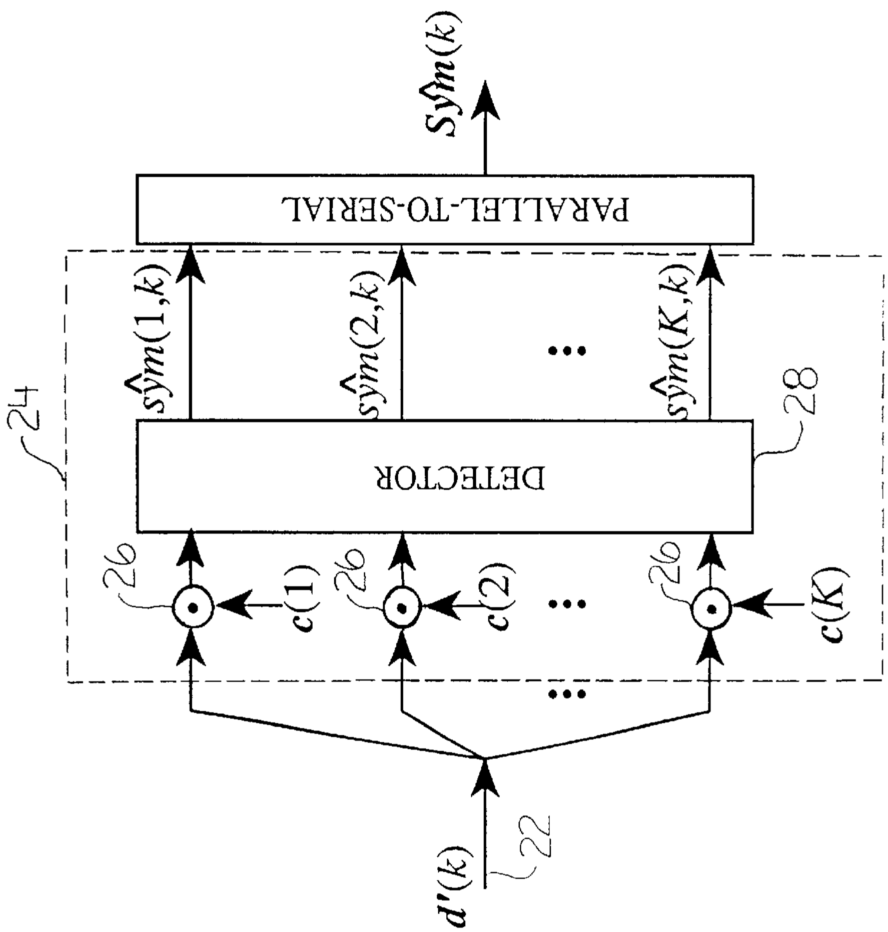

$S\hat{y}m(k)$
PARALLEL-TO-SERIAL
$s\hat{y}m(1,k)$
$s\hat{y}m(2,k)$
$s\hat{y}m(K,k)$
DETECTOR
28
24
26
$c(1)$
$c(2)$
$c(K)$
$d'(k)$
22

FIGURE 2

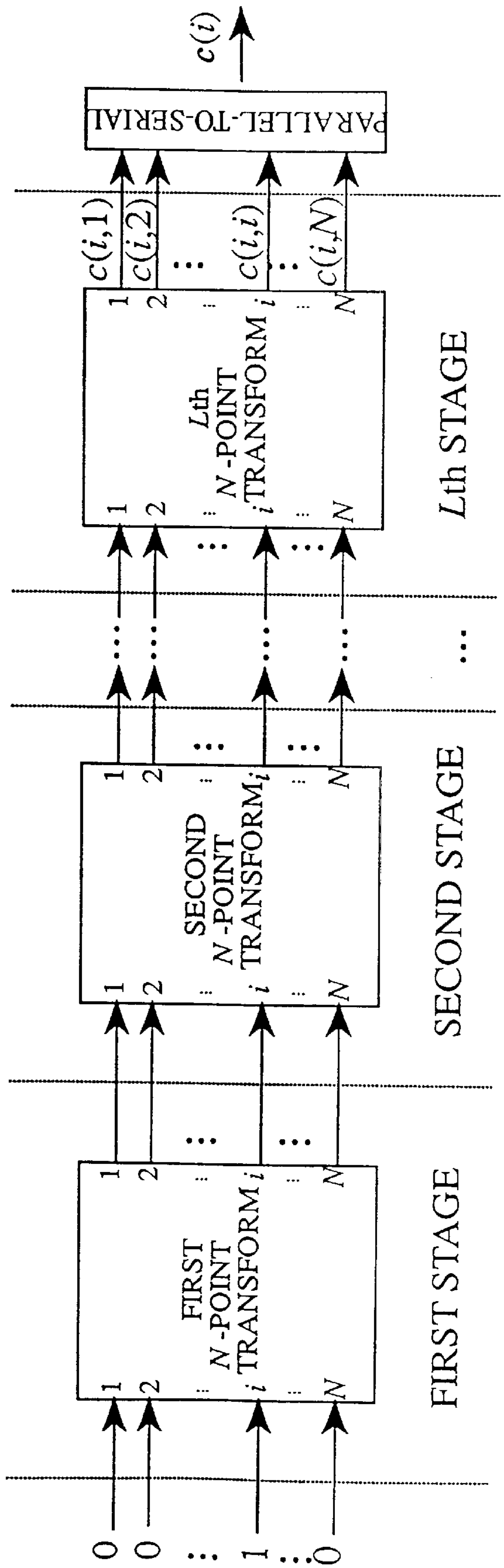

c(i)
PARALLEL-TO-SERIAL
c(i,1)
c(i,2)
c(i,i)
c(i,N)
Lth N-POINT TRANSFORM
Lth STAGE
SECOND N-POINT TRANSFORM
SECOND STAGE
FIRST N-POINT TRANSFORM
FIRST STAGE

FIGURE 3

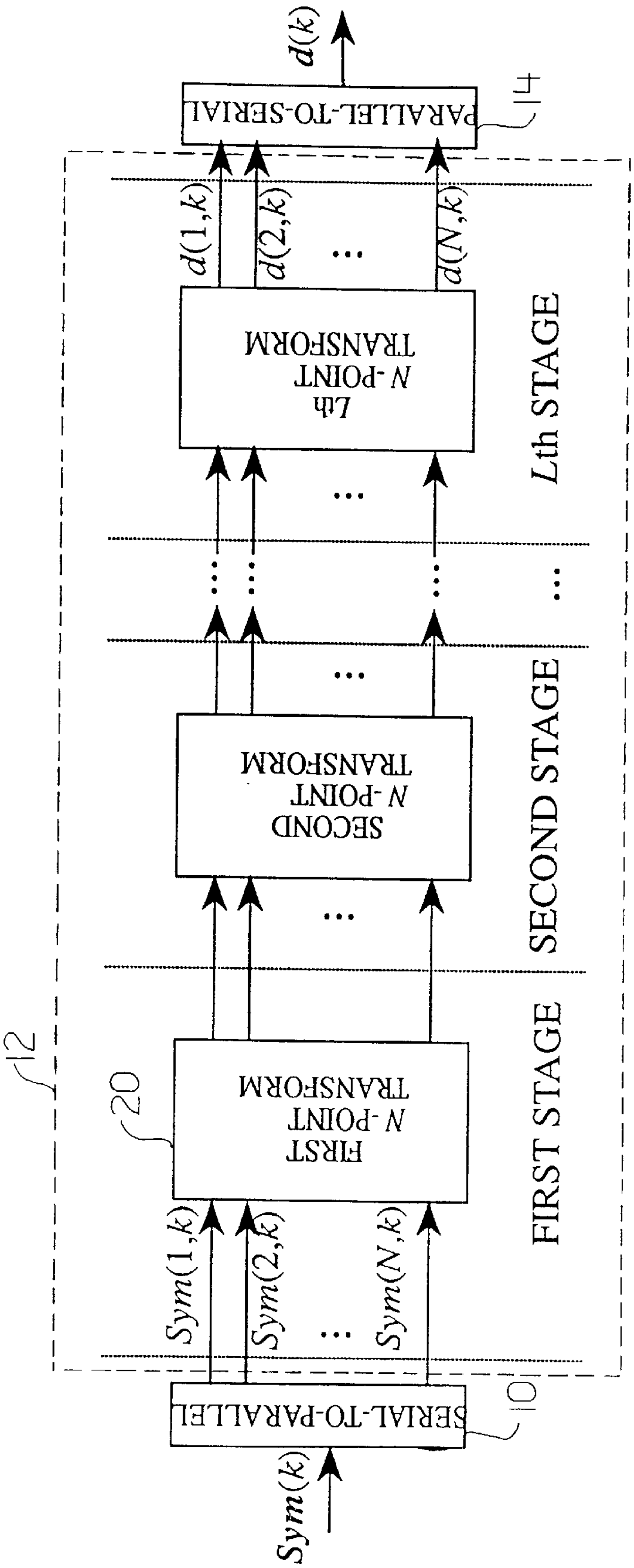
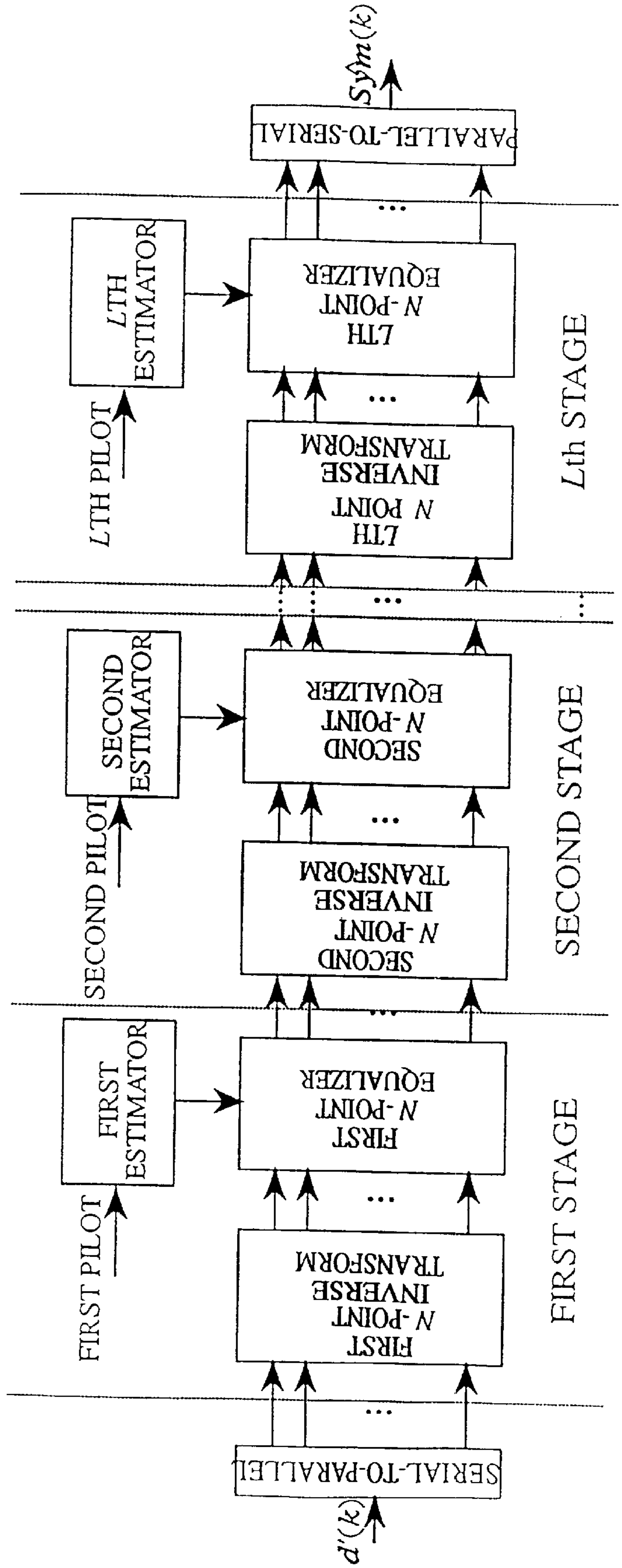

d(k)
PARALLEL-TO-SERIAL
14
d(1,k)
d(2,k)
...
d(N,k)
Lth
N-POINT
TRANSFORM
Lth STAGE
SECOND
N-POINT
TRANSFORM
SECOND STAGE
FIRST
N-POINT
TRANSFORM
FIRST STAGE
12
20
Sym(1,k)
Sym(2,k)
Sym(N,k)
SERIAL-TO-PARALLEL
10
Sym(k)

FIGURE 4



$d'(k)$
SERIAL-TO-PARALLEL
FIRST N-POINT INVERSE TRANSFORM
FIRST N-POINT EQUALIZER
FIRST PILOT
FIRST ESTIMATOR
FIRST STAGE
SECOND N-POINT INVERSE TRANSFORM
SECOND N-POINT EQUALIZER
SECOND PILOT
SECOND ESTIMATOR
SECOND STAGE
LTH N POINT INVERSE TRANSFORM
LTH N-POINT EQUALIZER
LTH PILOT
LTH ESTIMATOR
Lth STAGE
PARALLEL-TO-SERIAL
$S\hat{y}m(k)$

FIGURE 5

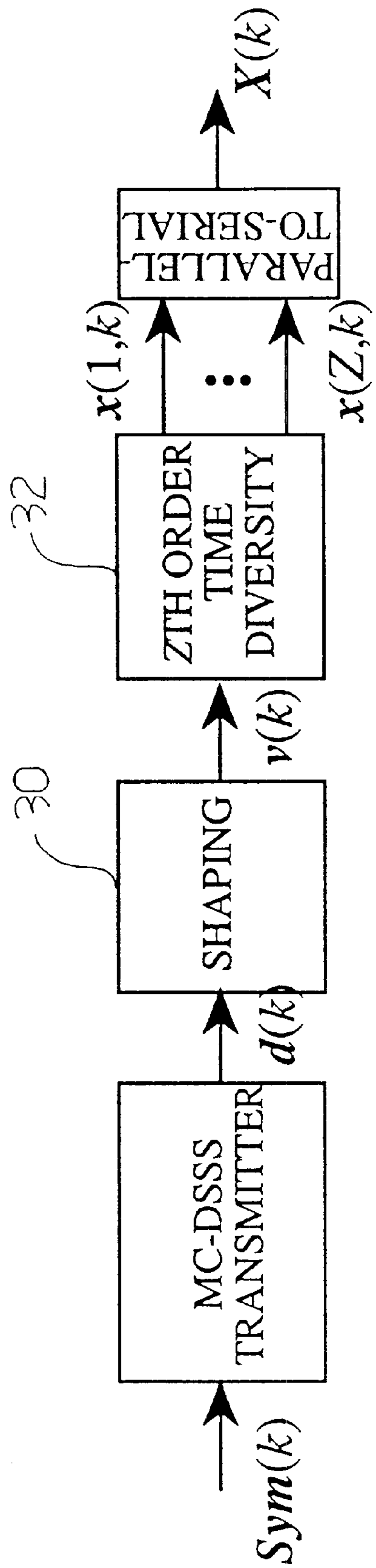

Sym(k)
MC-DSSS TRANSMITTER
d(k)
SHAPING
30
v(k)
ZTH ORDER TIME DIVERSITY
32
x(1,k)
x(Z,k)
PARALLEL-TO-SERIAL
X(k)

FIGURE 6

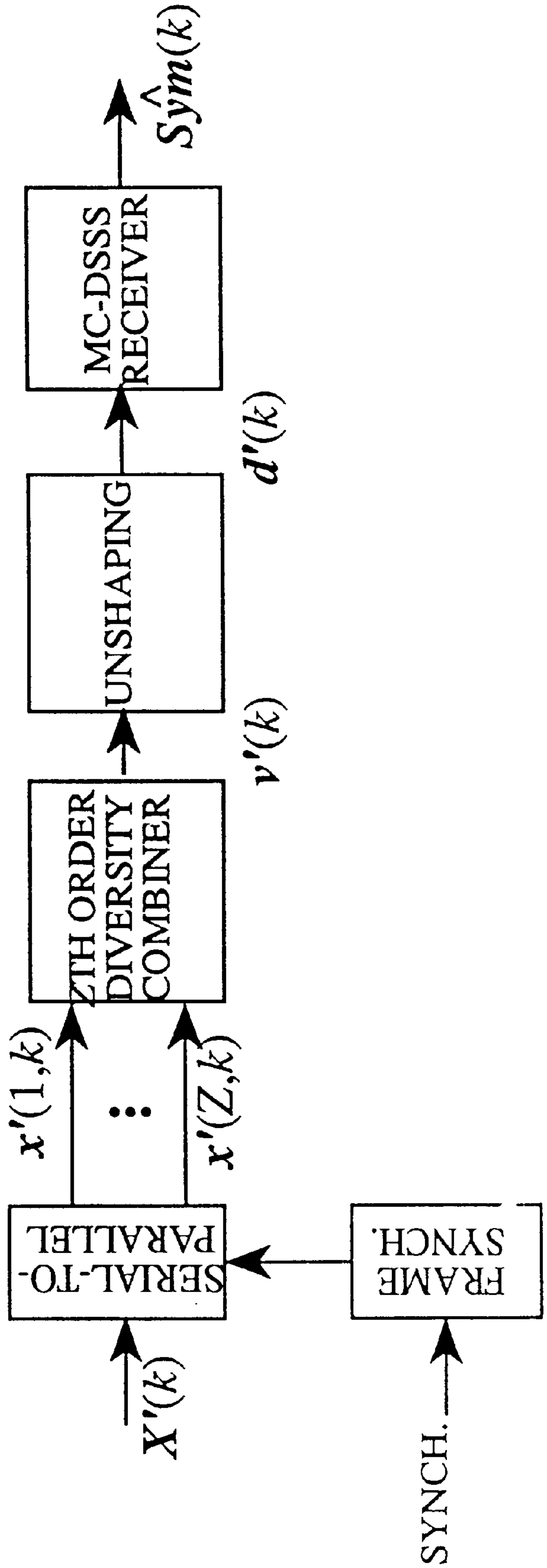

X'(k)
SERIAL-TO-PARALLEL
SYNCH.
FRAME SYNCH.
x'(1,k)
x'(Z,k)
ZTH ORDER DIVERSITY COMBINER
v'(k)
UNSHAPING
d'(k)
MC-DSSS RECEIVER
Sym(k)

FIGURE 7

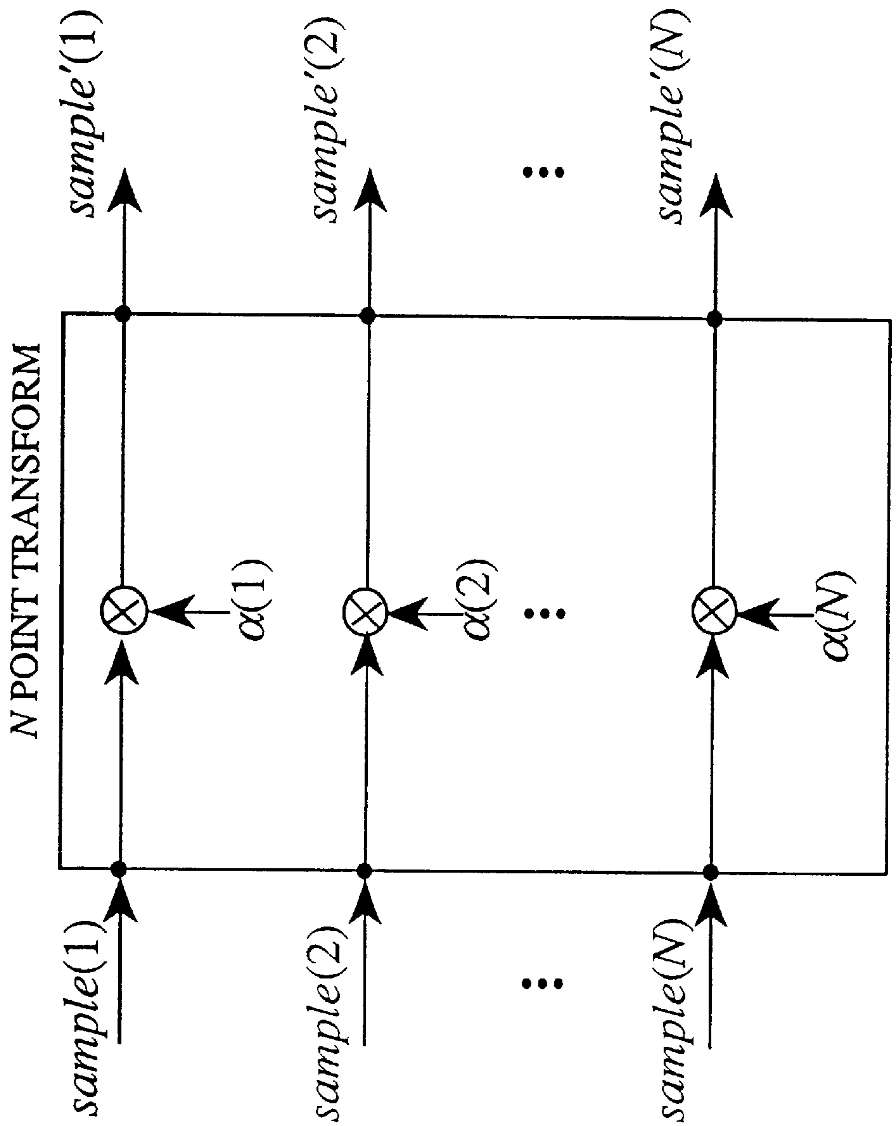

N POINT TRANSFORM
sample'(1)
sample'(2)
sample'(N)
α(1)
α(2)
α(N)
sample(1)
sample(2)
sample(N)

FIGURE 8

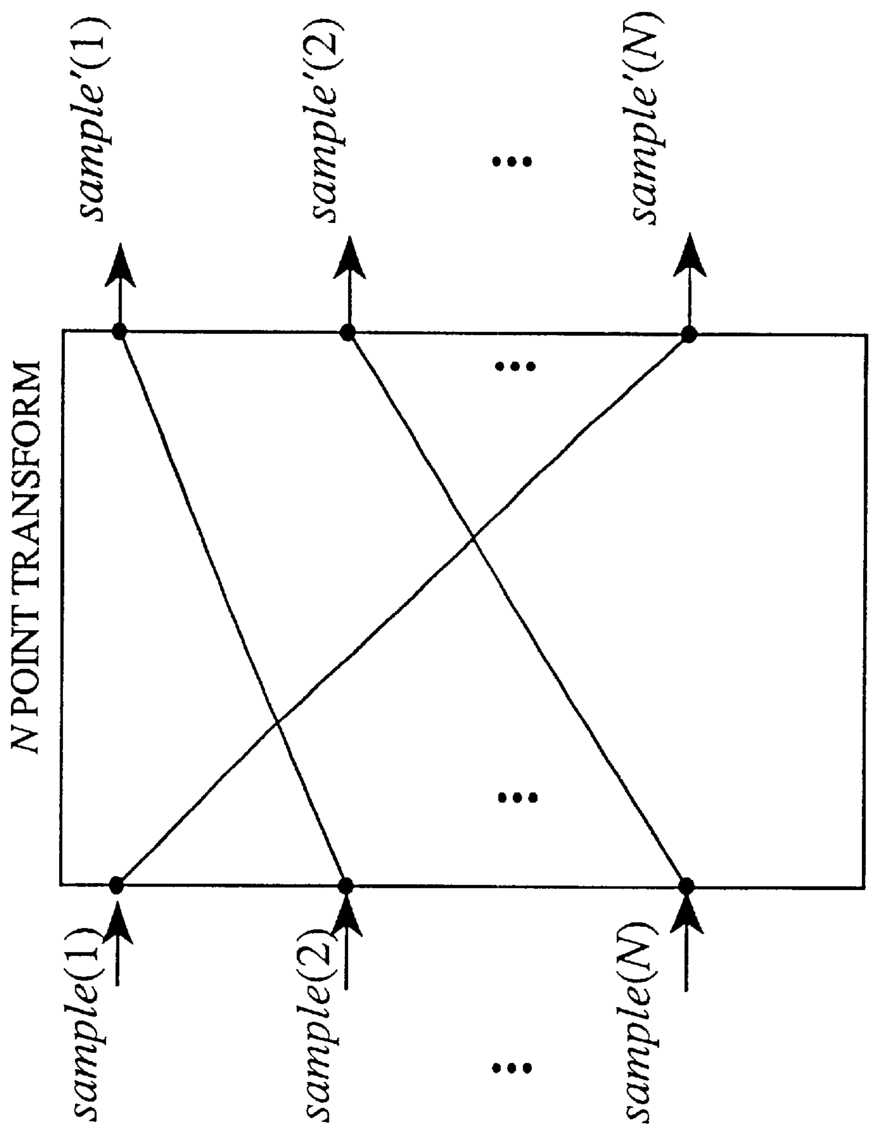

N POINT TRANSFORM
sample(1)
sample(2)
...
sample(N)
sample'(1)
sample'(2)
...
sample'(N)

FIGURE 9

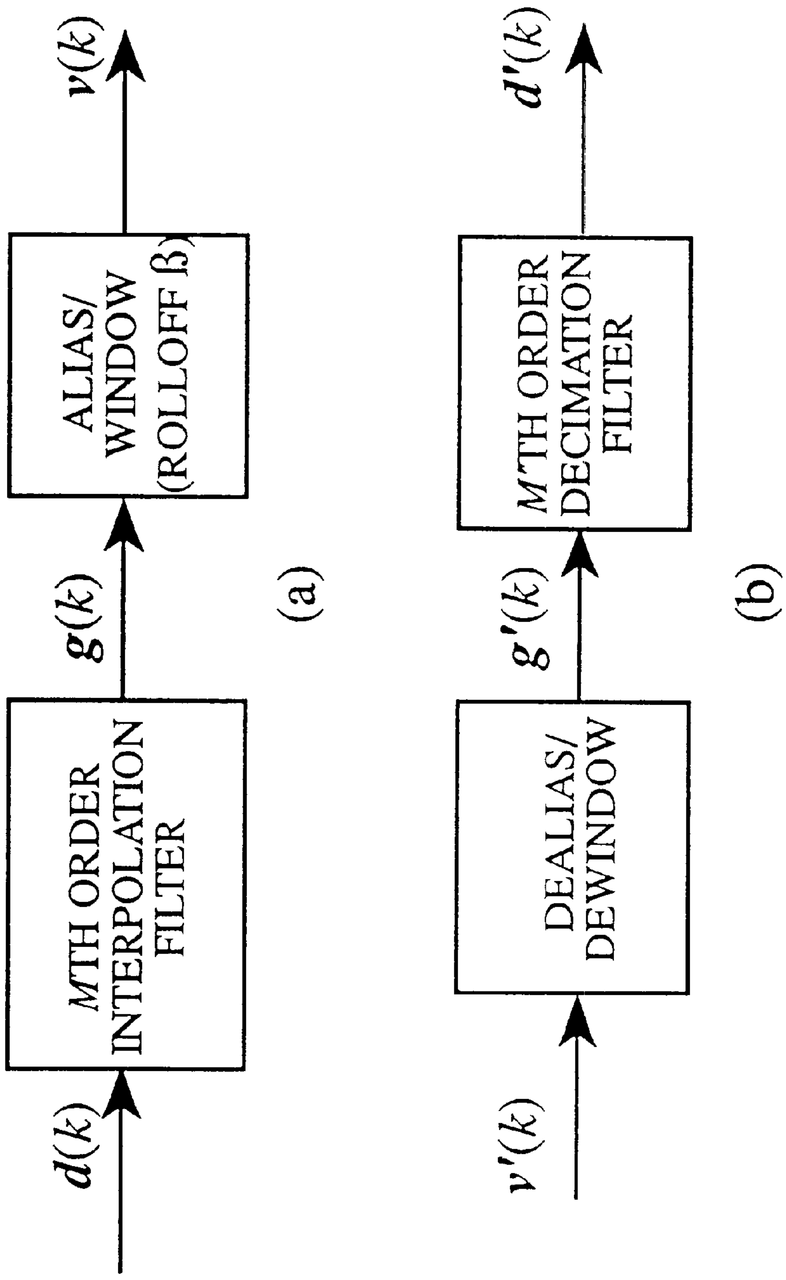

d(k)
MTH ORDER INTERPOLATION FILTER
g(k)
ALIAS/ WINDOW (ROLLOFF β)
v(k)
(a)
v'(k)
DEALIAS/ DEWINDOW
g'(k)
MTH ORDER DECIMATION FILTER
d'(k)
(b)

FIGURE 10

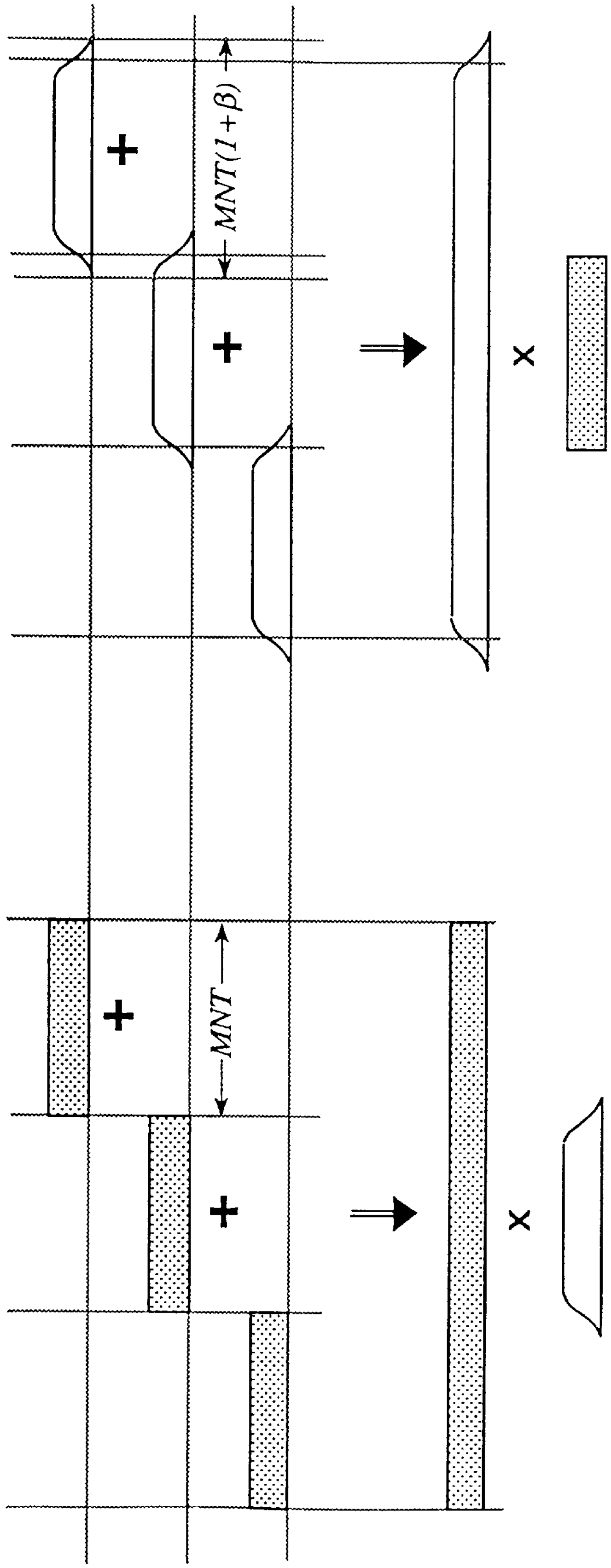


FIGURE 11

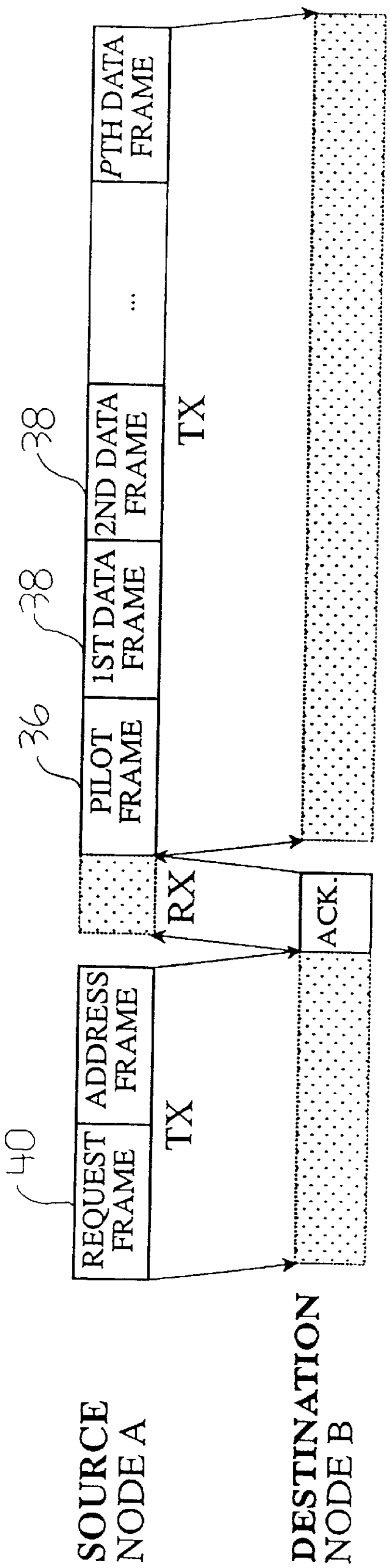

SOURCE NODE A
DESTINATION NODE B
40
REQUEST FRAME
ADDRESS FRAME
TX
ACK.
RX
36
PILOT FRAME
38
1ST DATA FRAME
38
2ND DATA FRAME
TX
PTH DATA FRAME

FIGURE 12

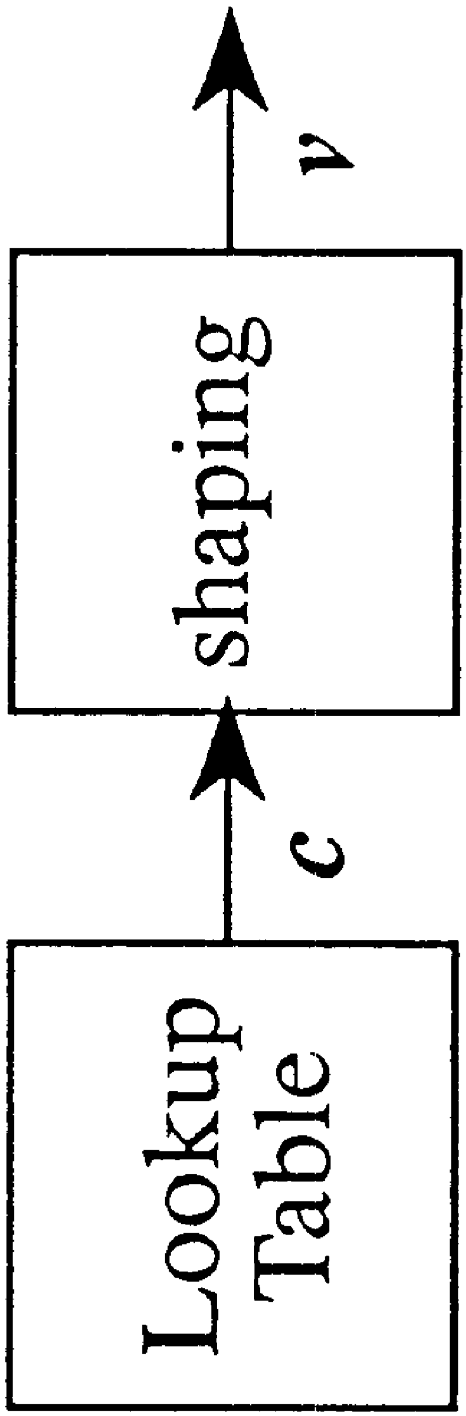


FIGURE 13

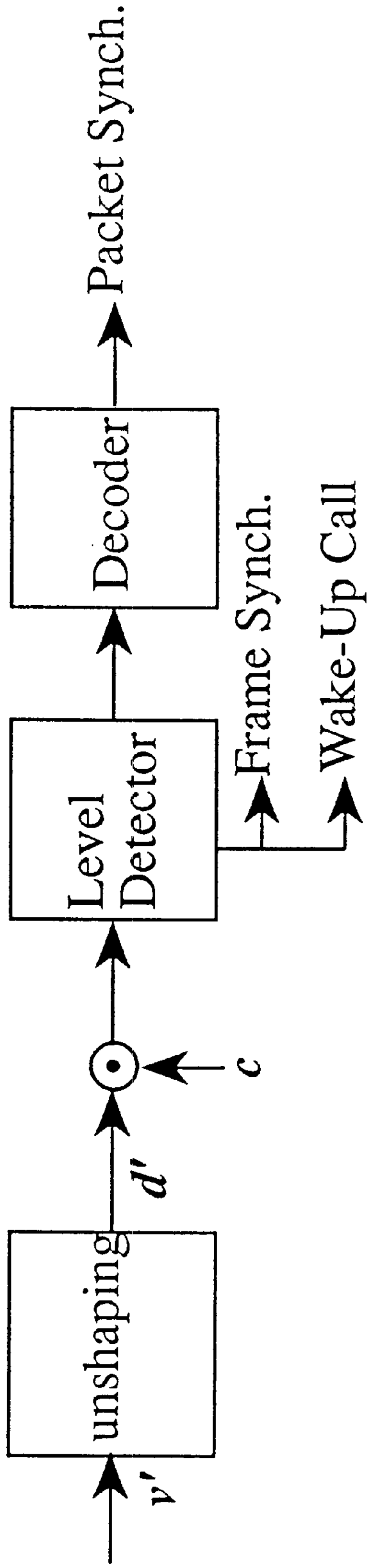

v'
unshaping
d'
c
Level Detector
Frame Synch.
Wake-Up Call
Decoder
Packet Synch.

FIGURE 14

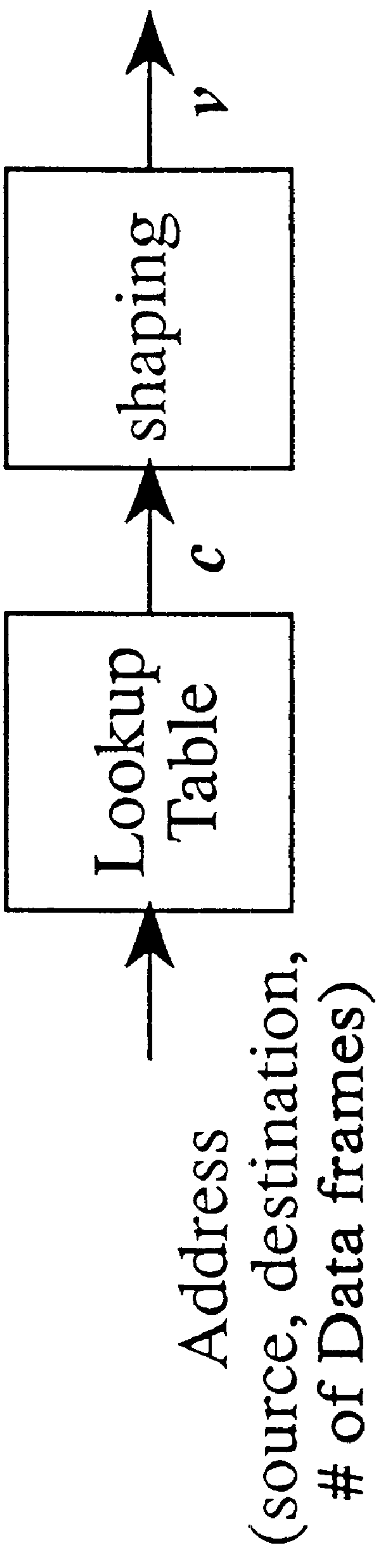

Address
(source, destination,
# of Data frames)
Lookup
Table
c
shaping
v

FIGURE 15

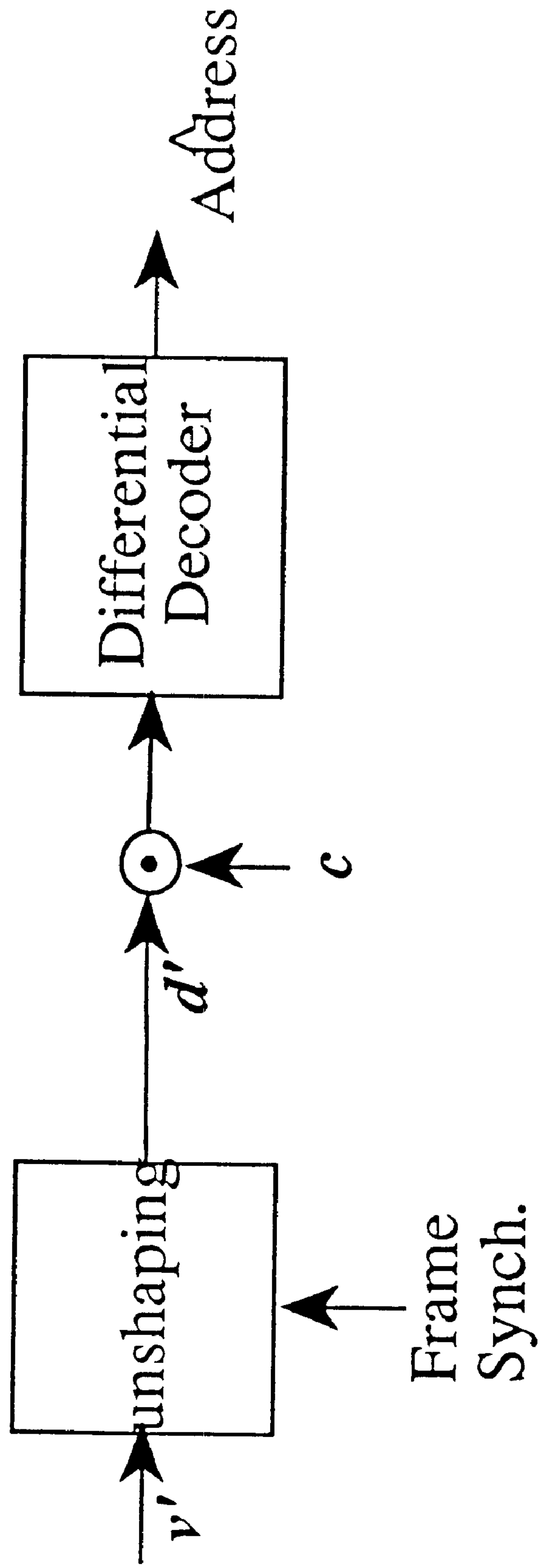


FIGURE 16

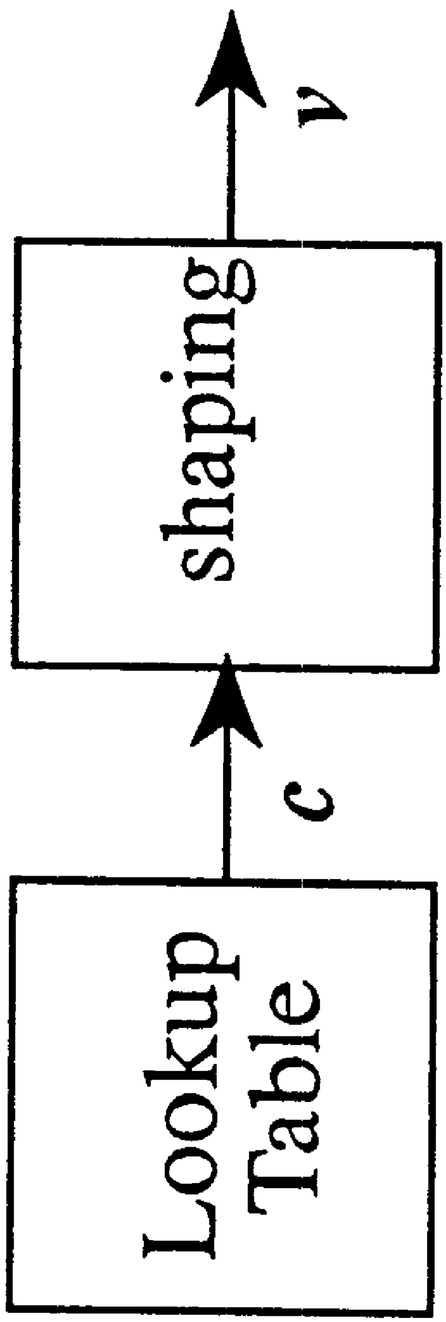


FIGURE 17

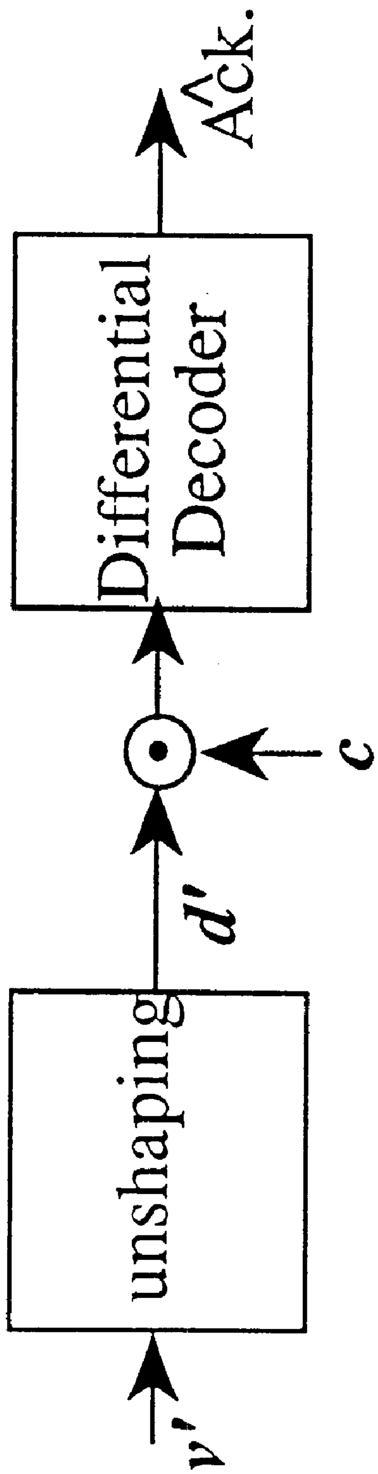


FIGURE 18

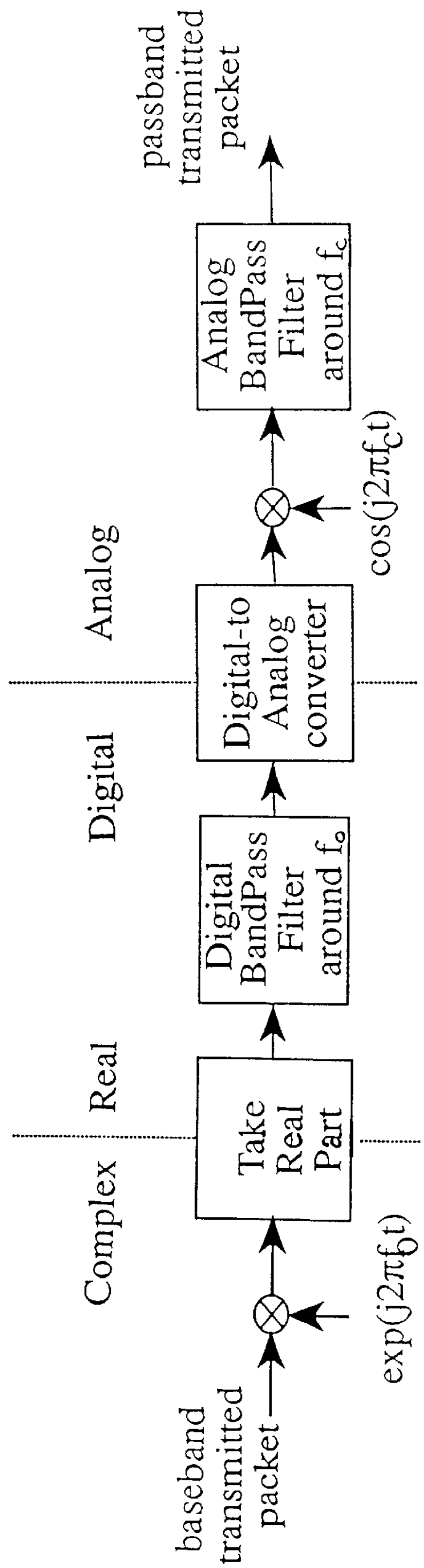

baseband transmitted packet
exp(j2πf₀t)
Complex
Real
Take Real Part
Digital BandPass Filter around f₀
Digital
Analog
Digital-to Analog converter
cos(j2πf_c t)
Analog BandPass Filter around f_c
passband transmitted packet

FIGURE 19

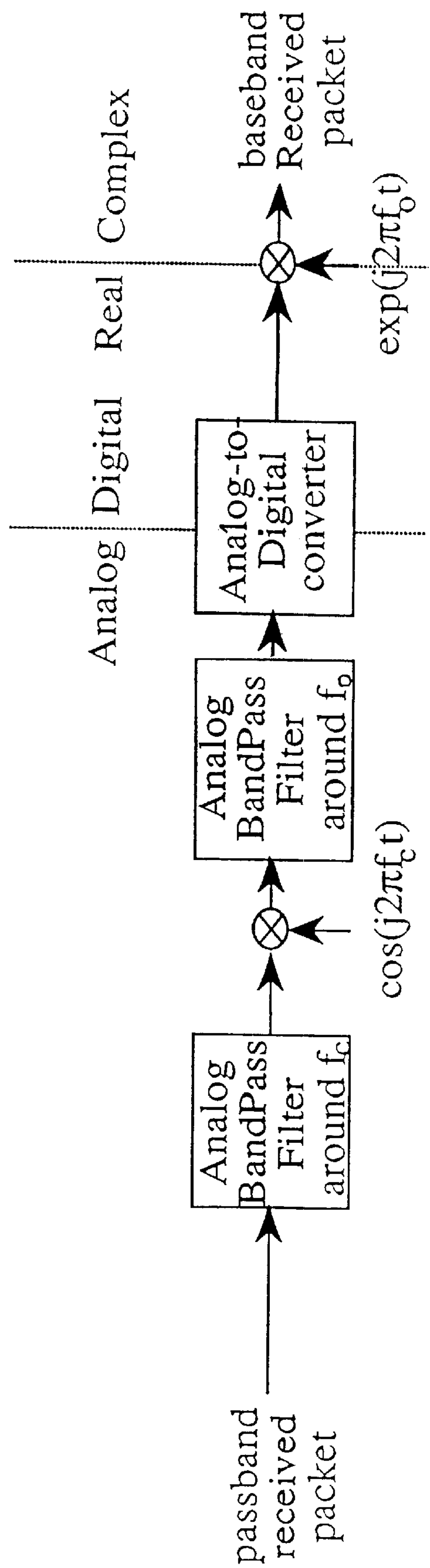

passband received packet
Analog BandPass Filter around f_c
$\cos(j2\pi f_c t)$
Analog BandPass Filter around f_o
Analog-to-Digital converter
Analog
Digital
Real
Complex
$\exp(j2\pi f_o t)$
baseband Received packet

FIGURE 20

MULTICODE DIRECT SEQUENCE SPREAD SPECTRUM

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

This application is a REISSUE of Ser. No. 08/186,784 filed Jan. 24, 1994 is a continuation-in-part of U.S. application Ser. No. 07/861,725 filed Mar. 31, 1992, now U.S. Pat. No. 5,282,222, the benefit of the filing date of which is hereby claimed under 35 U.S.C. §120.

FIELD OF THE INVENTION

The invention deals with the field of multiple access communications using Spread Spectrum modulation. Multiple access can be classified as either random access, polling, TDMA, FDMA, CDMA or any combination thereof. Spread Spectrum can be classified as Direct Sequence, Frequency-Hopping or a combination of the two.

BACKGROUND OF THE INVENTION

Commonly used spread spectrum techniques are Direct Sequence Spread Spectrum (DSSS) and Code Division Multiple Access (CDMA) as explained in Chapter 8 of "Digital Communication" by J. G. Proakis, Second Edition, 1991, McGraw Hill, DSSS is a communication scheme in which information bits are spread over code bits (generally called chips). It is customary to use noise-like codes called pseudo random noise (PN) sequences. These PN sequences have the property that their auto-correlation is almost a delta function and their cross-correlation with other codes is almost null. The advantages of this information spreading are:

1. The transmitted signal can be buried in noise and thus has a low probability of intercept.
2. The receiver can recover the signal from interferers (such as other transmitted codes) with a jamming margin that is proportional to the spreading code length.
3. DSSS codes of duration longer than the delay spread of the propagation channel can lead to multipath diversity implementable using a Rake receiver.
4. The FCC and the DOC have allowed the use of unlicensed low power DSSS systems of code lengths greater than or equal to 10 in some frequency bands (the ISM bands).

It is the last advantage (i.e., advantage 4. above) that has given much interest recently to DSSS.

An obvious limitation of DSSS systems is the limited throughput they can offer. In any given bandwidth, B, a code of length N will reduce the effective bandwidth to B/N. To increase the overall bandwidth efficiency, system designers introduced Code Division Multiple Access (CDMA) where multiple DSSS communication links can be established simultaneously over the same frequency band provided each link uses a unique code that is noise-like. CDMA problems are:

1. The near-far problem: a transmitter "near" the receiver sending a different code than the receiver's desired code produces in the receiver a signal comparable with that of a "far" transmitter sending the desired code.
2. Synchronization of the receiver and the transmitter is complex (especially) if the receiver does not know in advance which code is being transmitted.

SUMMARY OF THE INVENTION

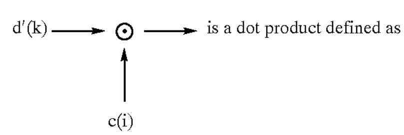
We have recognized that low power DSSS systems complying with the FCC and the DOC regulations for the ISM bands would be ideal communicators provided the problems of CDMA could be resolved and the throughput could be enhanced. To enhance the throughput, we allow a single link (i.e., a single transceiver) to use more than one code at the same time. To avoid the near-far problem only one transceiver transmits at a time. In this patent, we present Multi-Code Direct Sequence Spread Spectrum (MC-DSSS) which is a modulation scheme that assigns up to N codes to an individual transceiver where N is the number of chips per DSSS code. When viewed as DSSS, MC-DSSS requires up to N correlators (or equivalently up to N Matched Filters) at the receiver with a complexity of the order of N^2 operations. When N is large, this complexity is prohibitive. In addition, a nonideal communication channel can cause InterCode Interference (ICI), i.e., interference between the N DSSS codes at the receiver. In this patent, we introduce new codes, which we refer to as "MC" codes. Such codes allow the information in a MC-DSSS signal to be decoded in a sequence of low complexity parallel operations while reducing the ICI. In addition to low complexity decoding and ICI reduction, our implementation of MC-DSSS using the MC codes has the following advantages:

1. It does not require the stringent synchronization DSSS requires. Conventional DSSS systems requires synchronization to within a fraction of a chip whereas MC-DSSS using the MC codes requires synchronization to within two chips.
2. It does not require the stringent carrier recovery DSSS requires. Conventional DSSS requires the carrier at the receiver to be phase locked to the received signal whereas MC-DSSS using the MC codes does not require phase locking the carriers. Commercially available crystals have sufficient stability for MC-DSSS.
3. It is spectrally efficient.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic showing for the Baseband Transmitter for the xth MC-DSSS frame: d(k)=[d(1,x) d(2,x) . . . d(N,k)] where c(i)=[c(1,i) c(2,i)] is the ith code and Sym (k)=[sym(1,k) sym(N,k)] is the kth information-bearing vector containing N symbols.

FIG. **2** is a schematic showing a Baseband Receiver for the kth received MC-DSSS frame: d'(k)=[d'(1,k) d'(2,k) . . . d'(N,k)] where c(i)=[c(1,i) c(2,i) . . . c(N,i)] is the ith code, $Sy\hat{m}(k)=[sy\hat{m}(1,k)\ sy\hat{m}(2,k) \ldots sy\hat{m}(N,k)]$ is the estimate of the Kth information-bearing vector Sym(k) and



$$d'(k) \odot c(i) = c(1,i)d'(1,k) = c(2,i)d'(2,k) + \ldots + c(N,i)d'(N,N).$$

FIG. **3** is a schematic showing of the ith MC code c(i)=[c(i,1) c(i,2) . . . c(i,NO) where i can take one of the N values: 1,2, . . . N corresponding to the position of the single '1' at the input of the first N-point transform.

FIG. **4** is a schematic showing the alternate transmitter for the kth MC-DSSS frame: d(k)=[d(1,k), d(2,k) . . . d(N,k)] using the MC codes generated in FIG. **3** where Sym(k)=[Sym(1,k)Sym(2k) . . . Sym(N,k)] is the kth information-bearing vector contacting N symbols.

FIG. **5** is the alternate receiver for the kth received MC-DSSS frame d'(k)=[d'(1k)d'(2,K) . . .d'(N,k)] using MC codes generated in FIG. **3** where $Sy\hat{m}(k)=[sy\hat{m}(1,k)\ sy\hat{m}(2k) \ldots sy\hat{m}(N,k)]$ is the estimate of the information-bearing vetor Sym(k).

FIG. **6** is a schematic showing the Baseband Transmitter of the kth Data Frame X(k) where Sym(N)=[sym(1,k) sym (2,k) . . . sym(N,k)] is the kth information-bearing vector d(k)=[c(1,k) d(2,k) . . . d(N,k)] is the kth MC-DSSS frame v(k)=[v(1,k) v(2,k) . . . v((1+β)MN,k)], β∊(0,1), M=1,2,3 . . . and X(k)=[x(1k) x(2,k)], Z=Z=1, 2, 3, ...

FIG. **7** is a schematic showing the Baseband Receiver for the kth received Data Frame X'(k) where Sym̂(N)=[sym̂ (1,k)] sym̂(2,k) . . . sym̂(N,k)] is the estimate of the kth information-bearing vector d'(k)=[d'(1,k) d'(2k) . . . d'(N,k)] is the kth received MC-DSSS frame v'(k)=[v'(1,k) v(2k) . . . v'((1+β) MN,k)], B∊(0,1), M=1,2,3, . . . and X'(k)=[x'(1,k) x'(2,k) . . . r'(Z,k)], Z=1,2,3 . . . .

FIG. **8** is a schematic showing the Randomizer Transform (RT) where a (1) a (2) . . . a (N) are complex constants chosen randomly.

FIG. **9** is a schematic showing the Permutation Transform (PT).

FIG. **10** is a schematic showing (a) the shaping of a MC-DSSS frame and (b) the unshaping of a MC-DSSS frame where d(k)=[d(1,k) d(2,k) . . . d(N,k)] is the kth MC-DSSS frame g(k)=[g(1,k) g(2k) . . . g(MN,k)], M=1,2,3, . . . , v(k)=[v(1,k) v(2,k) . . . v((1+β) MN,k)], B∊(0,1) d'(k)=[d(1,k) d(2,k) . . . d(N,K)] is the kth received MC-DSSS frame g'(k)=[g'(1,k) g'(2,k) . . . g'(M'N,k)] and v'(k)=[v(1,k) v'(2,k) . . . v'((1+β) M'N,k)], M'=1,2,3, ...

FIG. **11** is a schematic showing (a) Description of the alias/window operation (b) Description of dealias/dewindow operation, where 1/T is the symbol rate.

FIG. **12** is a schematic showing the frame structure for data transmission from source (Node A) to destination (Node B).

FIG. **13** is a schematic showing the baseband transmitter for one request frame v where c=[c(1) c(2) . . . c(1)] is the DSSS code, v=[v(1) v(2) . . . v((1+β)MI)], β∊(0,1), M=1,2, . . . and I is the length of the DSSS code.

FIG. **14** is a schematic showing the baseband receiver for the received request frame where c=[c(1) c(2) . . . c(1)] is the DSSS code for the request frame, d'=[d(1) d(2) . . . d(1)] is the received request frame, v'=[v'(1) v'((1+β) MI)], β∊(0,1), M=1,2, . . . and l is the length of the DSSS code.

FIG. **15** is a schematic showing the baseband transmitter for one address frame where c=[c(1) c(2) . . . c(1)] is the CDMA code for the address frame, v=[v(1) v(2) . . . v(1+β) MI)], β∊(0,1), M=1,2, . . . and l' is the length of the CDMA code.

FIG. **16** is a schematic showing the baseband receiver the address where c=[c(1) c(2) . . . c(I')] is the CDMA code for the address frame, d'=[d(1) d(2) . . . d(I)] is the received address frame, v'[v'(1) v'(2) . . . v'((1+β) MI')], β∊(0,1), M=1,2, . . . and I' is the length of the CDMA code.

FIG. **17** is a schematic showing the baseband transmitter for Ack. Frame where c=[c(1) c(2) . . . c(I')] is the DSSS code for the Ack. frame, v=[v(1) v(2) . . . v((I+β) MI')] β∊(0,1), M=1,2,3, . . . and I' is the length of the DSSS code.

FIG. **18** is a schematic showing the baseband receiver for the ack. frame where c=[c(1) c(2) . . . c(I")] is the DSSS code for the Ack. frame, d'=[d(1) d(2) . . . d'(I")] is the received Ack. frame, v'=[v'(1) v(2) . . . v'(1+β) MI")], β∊(0,1), M=1,2, . . . and I" is the length of the DSSS code.

FIG. **19** is a schematic showing the passband transmitter for a packet where f_o is the IF frequency and f_o+f_c is the RF frequency.

FIG. **20** is a schematic showing the passband receiver for a packet where f_o is the IF frequency and f_o+f_c is the RF frequency.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS OF THE INVENTION

FIG. **1** illustrates the transmitter of the MC-DSSS modulation technique generating the kth MC-DSSS frame bearing N symbols of information. The symbols can be either analog or digital.

A converter **10** converts a stream of data symbols into plural sets of N data symbols each. A computing means **12** operates on the plural sets of N data symbols to produce modulated data symbols corresponding to an invertible randomized spreading of the stream of data symbols. A combiner **14** combines the modulated data symbols for transmission. The computing means shown in FIG. **1** includes a source **16** of N direct sequence spread spectrum code symbols and a modulator **18** to modulate each ith data symbol from each set of N data symbols with the I code symbol from the N code symbol to generate N modulated data symbols, and thereby spread each I data symbol over a separate code symbol.

FIG. **2** illustrates the receiver of the MC-DSSS modulation techniques accepting the kth MC-DSSS frame and generating estimates for the corresponding N symbols of information. The dot product in FIG. **2** can be implemented as a correlator. The detector can make either hard decisions or soft decisions.

A sequence of modulated data symbols is received at **22** in which the sequence of modulated data symbols has been generated by the transmitter such as is shown in FIG. **1** or **4**. A second computing means **24** operates on the sequence of modulated data symbols to produce an estimate of the second string of data symbols. The computing means **24** shown in FIG. **2** includes a correlator **26** for correlating each I modulated data symbol from the received sequence of modulated data symbols with the I code symbol from the set of N code symbols and a detector **28** for detecting an estimate of the data symbols from output of the correlator **26**.

FIG. **3** illustrates the code generator of the MC codes. Any one of the P N-point transforms in FIG. **3** consists of a reversible transform to the extent of the available arithmetic precision. In other words, with finite precision arithmetic, the transforms are allowed to add a limited amount of irreversible error.

One can use the MC-DSSS transmitter in FIG. **1** and the MC-DSSS receiver in FIG. **2** together with the MC codes generated using the code generator in FIG. **3** in order to implement MC-DSSS using the MC codes.

An alternative transmitter to the one in FIG. **1** using the MC codes in FIG. **3** is shown in FIG. **4**.

The alternative transmitter shown in FIG. **4** includes a transformer **20** for operating on each set of N data symbols to generate N modulated data symbols as output. A series of transforms are shown.

An alternative receiver to the one in FIG. **2** using the MC codes in FIG. **3** is shown in FIG. **5**. L pilots are required in FIG. **5** for equalization.

Both transmitters in FIGS. **1** and **4** allow using shaper **30** in diversity module **32** shaping and time diversity of the MC-DSSS signal as shown in FIG. **6**. We will refer to the MC-DSSS frame with shaping and time diversity as a Data frame.

Both receivers in FIGS. **2** and **5** allow diversity combining followed by the unshaping of the Data frame as shown in FIG. **7**. A Synch. is required in FIG. **7** for frame synchronization.

In addition to the Data frames, we need to transmit (1) all of the L pilots used in FIG. **5** to estimate and equalize for the various types of channel distortions, (2) the Synch. signal used in FIG. **7** for frame synchronization, and (3) depending on the access technique employed, the source address, destination address and number of Data frames. We will refer to the combination of all transmitted frames as a packet.

PREFERRED EMBODIMENTS OF THE INVENTION

Examples of the N-point transforms in FIG. **3** are a Discrete Fourier Transform (DFT), a Fast Fourier Transform

(FFT), a Walsh Transform (WT), a Hilbert Transform (HT), a Randomizer Transform (RT) as the one illustrated in FIG. **8**, a Permutator Transform (PT) as the one illustrated in FIG. **9**, an Inverse DFT (IDFT), an Inverse FFT (IFFT), an Inverse WT (IWT), an Inverse HT (IHT), an Inverse RT (IRT), an Inverse PT (IPT), and any other reversible transform. When L=2 with the first N-point transform being a DFT and the second being a RT, we have a system identical to the patent: "Method and Apparatus for Multiple Access between Transceivers in Wireless Communications using OFDM Spread Spectrum" by M. Fattouche and H. Zaghloul, filed in the U.S. Pat Office in Mar. 31, 1992, Ser. No. 07/861,725.

Preferred shaping in FIG. **6** consists of an Mth order interpolation filter followed by an alias/window operation as shown in FIG. **10**a. The Alias/window operation is described in FIG. **11**a where a raised-cosine pulse of rolloff β is applied. The interpolation filter in FIG. **10**a can be implemented as an FIR filter or as an NM-point IDFT where the first N(M−1)/2 points and the last N(M−1)/2 points at the input of the IDFT are zero. Preferred values of M are 1,2,3 and 4.

Preferred unshaping in FIG. **7** consists of a dealias/dewindow operation followed by a decimation filter as shown in FIG. **10**b. The dealias/dewindow operation is described in FIG. **11**b.

Time Diversity in FIG. **6** can consist of repeating the MC-DSSS frame several times. It can also consist of repeating the frame several times then complex conjugating some of the replicas, or shifting some of the replicas in the frequency domain in a cyclic manner.

Diversity combining in FIG. **7** can consist of cophasing, selective combining, Maximal Ratio combining or equal gain combining.

In FIG. **5**, L pilots are used to equalize the effects of the channel on each information-bearing data frame. The pilot frames can consist of Data frames of known information symbols to be sent either before, during or after the data, or of a number of samples of known values inserted within two transformations in FIG. **4**. A preferred embodiment of the pilots is to have the first pilot consisting of a number of frames of known information symbols. The remaining pilots can consist of a number of known information symbols between two transforms. The L estimators can consist of averaging of the pilots followed by either a parametric estimation or a nonparametric one similar to the channel estimator in the patent: "Method and Apparatus for Multiple Access between Transceivers in Wireless Communications using OFDM Spread Spectrum" by M. Fattouche and H. Zaghloul, filed in the U.S. Pat Office in Mar. 31, 1992, Ser. No. 07/861,725.

When Node A intends to transmit information to Node B, a preferred embodiment of a packet is illustrated in FIG. **12**: a Request frame **40**, an Address frame, an Ack. frame, a Pilot frame **36** and a number of Data frames **38**. The Request frame is used (1) as a wake-up call for all the receivers in the band, (2) for frame synchronization and (3) for packet synchronization. It can consist of a DSSS signal using one PN code repeated a number of times and ending with the same PN code with a negative polarity. FIGS. **13** and **14** illustrate the transmitter and the receiver for the Request frame respectively. In FIG. **14**, the dot product operation can be implemented as a correlator with either hard or soft decision (or equivalently as a filter matched to the PN code followed by a sample/hold circuit). The Request frame receiver is constantly generating a signal out of the correlator. When the signal is above a certain threshold using the level detector, (1) a wake-up call signal is conveyed to the portion of the receiver responsible for the Address frame and (2) the frames are synchronized to the wake-up call. The

packet is then synchronized to the negative differential correlation between the last two PN codes in the Request frame using a decoder as shown in FIG. **14**.

The Address frame can consist of a CDMA signal where one out of a number of codes is used at a time. The code consists of a number of chips that indicate the destination address, the source address and/or the number of Data frames. FIGS. **15** and **16** illustrate the transmitter and the receiver for the Address frame respectively. Each receiver differentially detects the received Address frame, then correlates the outcome with it is own code. If the output of the correlator is above a certain threshold, the receiver instructs its transmitter to transmit an Ack. Otherwise, the receiver returns to its initial (idle) state.

The Ack. frame is a PN code reflecting the status of the receiver, i.e. whether it is busy or idle. When it is busy, Node A aborts its transmission and retries some time later. When it is idle, Node A proceeds with transmitting the Pilot frame and the Data frames. FIGS. **17** and **18** illustrate the transmitter and the receiver for the Address frame respectively.

An extension to the MC-DSSS modulation technique consists of passband modulation where the packet is up-converted from baseband to RF in the transmitter and later down-converted from RF to baseband in the receiver. Passband modulation can be implemented using IF sampling which consists of implementing quadrature modulation/demodulation in an intermediate Frequency between baseband and RF, digitally as shown in FIGS. **19** and **20** which illustrate the transmitter and the receiver respectively. IF sampling trades complexity of the analog RF components (at either the transmitter, the receiver or both) with complexity of the digital components. Furthermore, in passband systems carrier feed-through is often a problem implying that the transmitter has to ensure a zero dc component. Such a component reduces the usable bandwidth of the channel. In IF sampling the usable band of the channel does not include dc and therefore is the dc component is not a concern.

A further extension to the MC-DSSS modulation technique consists of using antenna Diversity in order to improve the Signal-to-Ratio level at the receiver. A preferred combining technique is maximal selection combining based on the level of the Request frame at the receiver.

We claim:

1. A transceiver for transmitting a first stream of data symbols, the transceiver comprising:

a converter for converting the first stream of data symbols into plural sets of N data symbols each;

first computing means for operating on the plural sets of N data symbols to produce modulated data symbols corresponding to an invertible randomized spreading of the first stream of data symbols; and

means to combine the modulated data symbols for transmission.

2. The transceiver of claim **1** in which the first computing means **[**includes**]** *comprises*:

a source of **[**N**]** *more than one and up to M* direct sequence spread spectrum **[**code symbols**]** *codes, where M is the number of chips per direct sequence spread spectrum code*; and

a modulator to modulate each **[**ith**]** data symbol from each set of **[**N**]** data symbols with **[**the ith**]** *a* code **[**symbol**]** from the **[**N code symbol**]** *up to M direct sequence spread spectrum codes* to generate **[**N**]** modulated data symbols, and thereby spread each **[**ith data symbol**]** *set of data symbols* over a separate code **[**symbol**]**.

3. The transceiver of claim **2** in which the **[**code symbols**]** *direct sequence spread spectrum codes* are generated by operation of a non-trivial **[**N point**]** transform on a sequence of input signals.

4. The transceiver of claim **1** in which the first computing means [includes] *comprises*:

a transformer for operating on each set of N data symbols to generate [N] modulated data symbols as output, the [N] modulated data symbols corresponding to spreading of each [ith] data symbol over a separate code [symbol] *selected from a set of more than one and up to M codes, where M is the number of chips per code; and*

means to combine the modulated data symbols for transmission.

5. The transceiver of claim **4** in which the transformer effectively applies a first transform selected from the group [comprising] *consisting of* a Fourier transform and a Walsh transform to the N data symbols.

6. The transceiver of claim **5** in which the first transform is a Fourier transform and it is followed by a randomizing transform.

7. The transceiver of claim **6** in which the first transform is a Fourier transform and it is followed by a randomizing transform and a second transform selected from the group [comprising] *consisting of* a Fourier transform and a Walsh transform.

8. The transceiver of claim **4** in which the transformer effectively applies a first inverse transform selected from the group [comprising] *consisting of* a randomizer transform, a Fourier transform and a Walsh transform to the N data symbols, followed by a first equalizer and a second inverse transform selected from the group [comprising] *consisting of* a Fourier transform and a Walsh transform.

9. The transceiver of claim **8** in which the second transform is followed by a second equalizer.

10. The transceiver of claim **1** further [including] *comprising*:

means for receiving a sequence of modulated data symbols, the modulated data symbols having been generated by invertible randomized spreading of a second stream of data symbols; *and*

second computing means for operating on the sequence of modulated data symbols to produce an estimate of the second stream of data symbols.

11. The transceiver of claim **10** further [including] *comprising* means to apply diversity to the modulated data symbols before transmission, and means to combine received diversity signals.

12. The transceiver of claim **10** in which the second computing means [includes] *comprises*:

a correlator for correlating each [ith] modulated data symbol from the received sequence of modulated data symbols with [the ith code symbol] *a code* from [the] *a* set of [N code symbols] *more than one and up to M codes, where M is the number of chips per code*; and

a detector for detecting an estimate of the data symbols from output of the correlator.

13. The transceiver of claim **10** in which the second computing means [includes] *comprises* an inverse transformer for regenerating an estimate of the [N] data symbols.

14. The transceiver of claim **1** further [including] *comprising* a shaper for shaping the combined modulated data symbols for transmission.

15. The transceiver of claim **1** further [including] *comprising* means to apply diversity to the combined modulated data symbols before transmission.

16. The transceiver of claim **1** in which the [N] data symbols include a pilot frame and a number of data frames, and is preceded by a request frame, wherein the request frame is used to wake up receiving transceivers, synchronize reception of the [N] data symbols and convey protocol information.

17. A transceiver for transmitting a first stream of data symbols and receiving a second stream of data symbols, the transceiver comprising:

a converter for converting the first stream of data symbols into plural sets of N data symbols each;

first computing means for operating on the plural sets of N data symbols to produce sets of [N] modulated data symbols corresponding to an invertible randomized spreading of each set of N data symbols over [N code symbols] *more than one and up to M direct sequence spread spectrum codes*;

means to combine the modulated data symbols for transmission;

means for receiving a sequence of modulated data symbols, the modulated data symbols having been generated by an invertible randomized spreading of a second stream of data symbols over [N code symbols] *more than one and up to M direct sequence spread spectrum codes*;

second computing means for operating on the sequence of modulated data symbols to produce an estimate of the second stream of data symbols; and

means to combine output from the second computing means.

18. The transceiver of claim **17** in which the first computing means [includes] *comprises*:

a source of [N] *the* direct sequence spread spectrum [code symbols] *codes*; and

a modulator to modulate each [ith] data symbol from each set of N data symbols with [the ith code symbol] *a code* from the [N code symbol] *up to M direct sequence spread spectrum codes* to generate [N] modulated data symbols, and thereby spread each [ith] data symbol over a separate *direct sequence spread spectrum* code [symbol].

19. The transceiver of claim **18** in which the [code symbols] *direct sequence spread spectrum codes* are generated by operation of plural non-trivial [N point] transforms on a random sequence of input signals.

20. The transceiver of claim **17** in which the first computing means [includes] *comprises*:

a transformer for operating on each set of N data symbols to generate [N] modulated data symbols as output, the [N] modulated data symbols corresponding to spreading of each [ith] data symbol over a separate code [symbol].

21. The transceiver of claim **17** in which the second computing means [includes] *comprises*:

a correlator for correlating each [ith] modulated data symbol from the received sequence of modulated data symbols with [the ith code symbol] *a code* from the [set of N code symbols] *up to M direct sequence spread spectrum codes*; and

a detector for detecting an estimate of the data symbols from the output of the correlator.

22. The transceiver of claim **17** in which the second computing means [includes] *comprises* an inverse transformer for regenerating an estimate of the N data symbols.

23. A method of exchanging data streams between a plurality of transceivers, the method comprising the steps of:

converting a first stream of data symbols into plural sets of N data symbols each;

operating on the plural sets of N data symbols to produce modulated data symbols corresponding to a spreading of the first stream of data symbols over [N code symbols] *more than one and up to M direct sequence spread spectrum codes*;

combining the modulated data symbols for transmission; and

transmitting the modulated data symbols from a first transceiver at a time when no other of the plurality of transceivers is transmitting.

24. The method of claim **23** in which the spreading is an invertible randomized spreading and operating on the plural sets of N data symbols [includes] *comprises* modulating each [ith] data symbol from each set of N data symbols with [the ith code symbol] *a code* from the [N code symbols] *up to M direct sequence spread spectrum codes* to generate [N] modulated data symbols, and thereby spread each [ith] data symbol over a separate code [symbol].

25. The method of claim **23** in which the spreading is an invertible randomized spreading and operating on the plural sets of N data symbols [includes] *comprises*:

transforming, by application of a transform, each set of N data symbols to generate [N] modulated data symbols as output.

26. The method of claim **25** in which transforming each set of N data symbols [includes] *comprises* applying to each set of N data symbols a randomizing transform and a transform selected from the group [comprising] *consisting of* a Fourier transform and a Walsh transform.

27. The method of claim **25** in which transforming each set of N data symbols [includes] *comprises* applying to each set of N data symbols a Fourier transform, a randomizing transform and a transform selected from the group [comprising] *consisting of* a Fourier transform and a Walsh transform.

28. The method of claim **25** in which transforming each set of N data symbols [includes] *comprises* applying to each set of N data symbols a first transform selected from the group [comprising] *consisting of* a Fourier transform and a Walsh transform, a randomizing transform and a second transform selected from the group [comprising] *consisting of* a Fourier transform and a Walsh transform.

29. The method of claim **23** further [including] *comprising* the step of:

receiving, at a transceiver distinct from the first transceiver, the sequence of modulated data symbols; and

operating on the sequence of modulated data symbols to produce an estimate of the first stream of data symbols.

30. The method of claim **29** in which operating on the sequence of modulated data symbols [includes] *comprises* the steps of:

correlating each [ith] modulated data symbol from the received sequence of modulated data symbols with [the ith code symbol from the set of N code symbols] *a code from the up to M direct sequence spread spectrum codes*; and

detecting an estimate of the first stream of data symbols from output of the correlator.

31. The method of claim **23** further [including] *comprising the step of* shaping the modulated data symbols before transmission.

32. The method of claim **23** further [including] *comprising the step of* applying diversity to the modulated data symbols before transmission.

33. A transceiver for transmitting a first stream of data symbols, the transceiver comprising:

a converter for converting the first stream of data symbols into plural sets of data symbols each;

first computing means for operating on the plural sets of data symbols to produce modulated data symbols corresponding to an invertible randomized spreading of the first stream of data symbols over more than one and up to M direct sequence spread spectrum codes, where each direct sequence spread spectrum code has M chips; and

means to combine the modulated data symbols for transmission.

34. The transceiver of claim 33 further comprising:

means for receiving a sequence of modulated data symbols, the modulated data symbols having been generated by invertible randomized spreading of a second stream of data symbols; and

second computing means for operating on the sequence of modulated data symbols to produce an estimate of the second stream of data symbols.

35. The transceiver of claim 34 further comprising means to apply diversity to the modulated data symbols before transmission, and means to combine received diversity signals.

36. The transceiver of claim 34 in which the second computing means comprises:

a correlator for correlating each modulated data symbol from the received sequence of modulated data symbols with a code from the set of up to M direct sequence spread spectrum codes; and

a detector for detecting an estimate of the data symbols from output of the correlator.

37. The transceiver of claim 34 in which the second computing means comprises an inverse transformer for regenerating an estimate of the data symbols.

38. The transceiver of claim 33 further comprising a shaper for shaping the combined modulated data symbols for transmission.

39. The transceiver of claim 33 further comprising means to apply diversity to the combined modulated data symbols before transmission.

40. The transceiver of claim 33 in which the data symbols include a pilot frame and a number of data frames, and is preceded by a request frame, wherein the request frame is used to wake up receiving transceivers, synchronize reception of the data symbols and convey protocol information.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : RE 37,802 E
DATED : July 23, 2002
INVENTOR(S) : M.T. Fattouche et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page,
Item [63], **Related U.S. Application Data**, insert in appropriate order

-- **Related U.S. Application Data**
[63] Continuation-in-part of U.S. application
No. 07/861,725, filed on Mar. 31, 1992, now Pat.
No. 5,282,222 --

Signed and Sealed this

Eleventh Day of March, 2003

JAMES E. ROGAN
Director of the United States Patent and Trademark Office

EXHIBIT B

US006192068B1

(12) **United States Patent**
Fattouche et al.

(10) **Patent No.: US 6,192,068 B1**
(45) **Date of Patent: *Feb. 20, 2001**

(54) **MULTICODE SPREAD SPECTRUM COMMUNICATIONS SYSTEM**

(75) Inventors: **Michel T. Fattouche**; **Hatim Zaghloul**; **Paul R. Milligan**; **David L. Snell**, all of Calgary (CA)

(73) Assignee: **Wi-Lan Inc.**, Alberta (CA)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Under 35 U.S.C. 154(b), the term of this patent shall be extended for 0 days.

(21) Appl. No.: **08/725,556**

(22) Filed: **Oct. 3, 1996**

(51) **Int. Cl.**[7] **H04B 15/00**

(52) **U.S. Cl.** **375/200**

(58) **Field of Search** 375/200, 206, 375/208, 204, 219; 370/342, 468, 335

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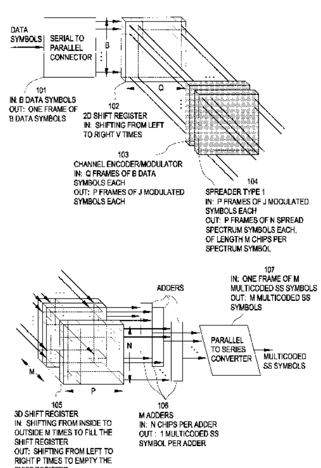
Primary Examiner—Chi H. Pham
Assistant Examiner—Khai Tran
(74) *Attorney, Agent, or Firm*—Christensen O'Connor Johnson Kindness PLLC

(57) **ABSTRACT**

MultiCode Spread Spectrum (MCSS) is a modulation scheme that assigns a number N of Spread Spectrum (SS) codes to an individual user where the number of chips per SS code is M. When viewed as Direct Sequence Spread Spectrum, MCSS requires up to N correlators (or equivalently up to N Matched Filters) at the receiver with a complexity of the order of NM operations. In addition, a non ideal communication channel can cause InterCode Interference (ICI), i.e. interference between the N SS codes. In this patent, we introduce three new types of MCSS. MCSS Type I allows the information in a MCSS signal to be detected using a sequence of partial corrrelations with a combined complexity of the order of M operations. MCSS Type II allows the information in a MCSS signal to be detected in a sequence of low complexity parallel operations which reduce the ICI. MCSS Type III allows the information in a MCSS signal to be detected using a filter suitable for ASIC implementation or on Digital Signal Processor, which reduces the effect of multipath. In addition to low complexity detection and reduced ICI, MCSS has the added advantage that it is spectrally efficient.

11 Claims, 22 Drawing Sheets



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Pupolin, Silvao, et al., "Performance Analysis Of Digital Radio Links With Nonlinear Transmit Amplifier And Data Predistorter With Memory," pp. 9.6.1–9.6.5.

Bingham, J.A.C., "Multicarrier Modulation for Data Transmission: An Idea Whose Time Has Come", *IEEE Communications Magazine,* pp. 5–14, May 1990.

Spracklen, C.T. and C. Smythe, "The Application of Code Division Multiplexing Techniques to Local Area Networks," pp. 767–770, May 1987.

* cited by examiner

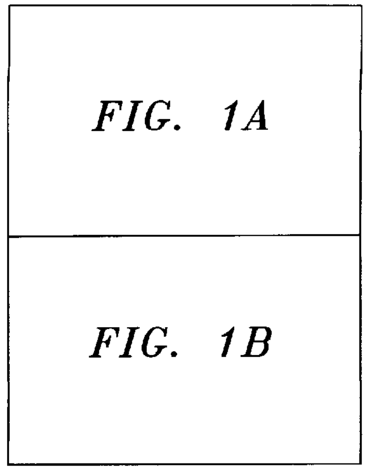


FIG. 1A
FIG. 1B

FIG. 1

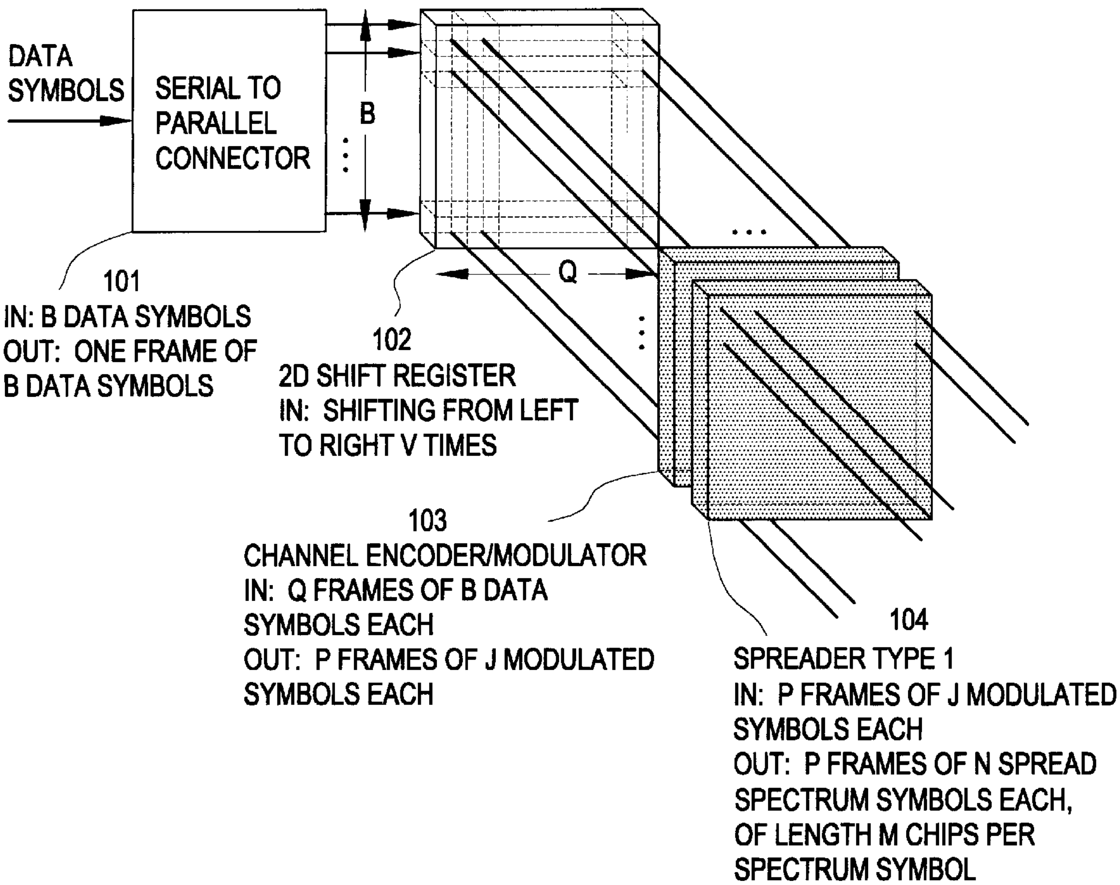
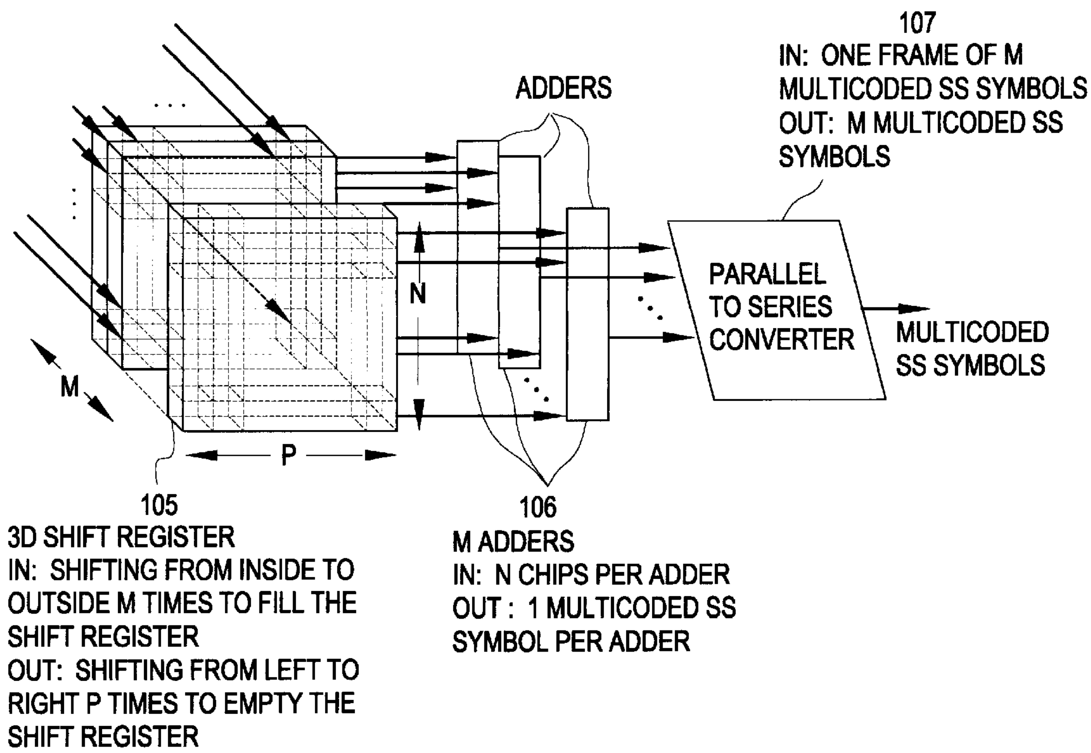
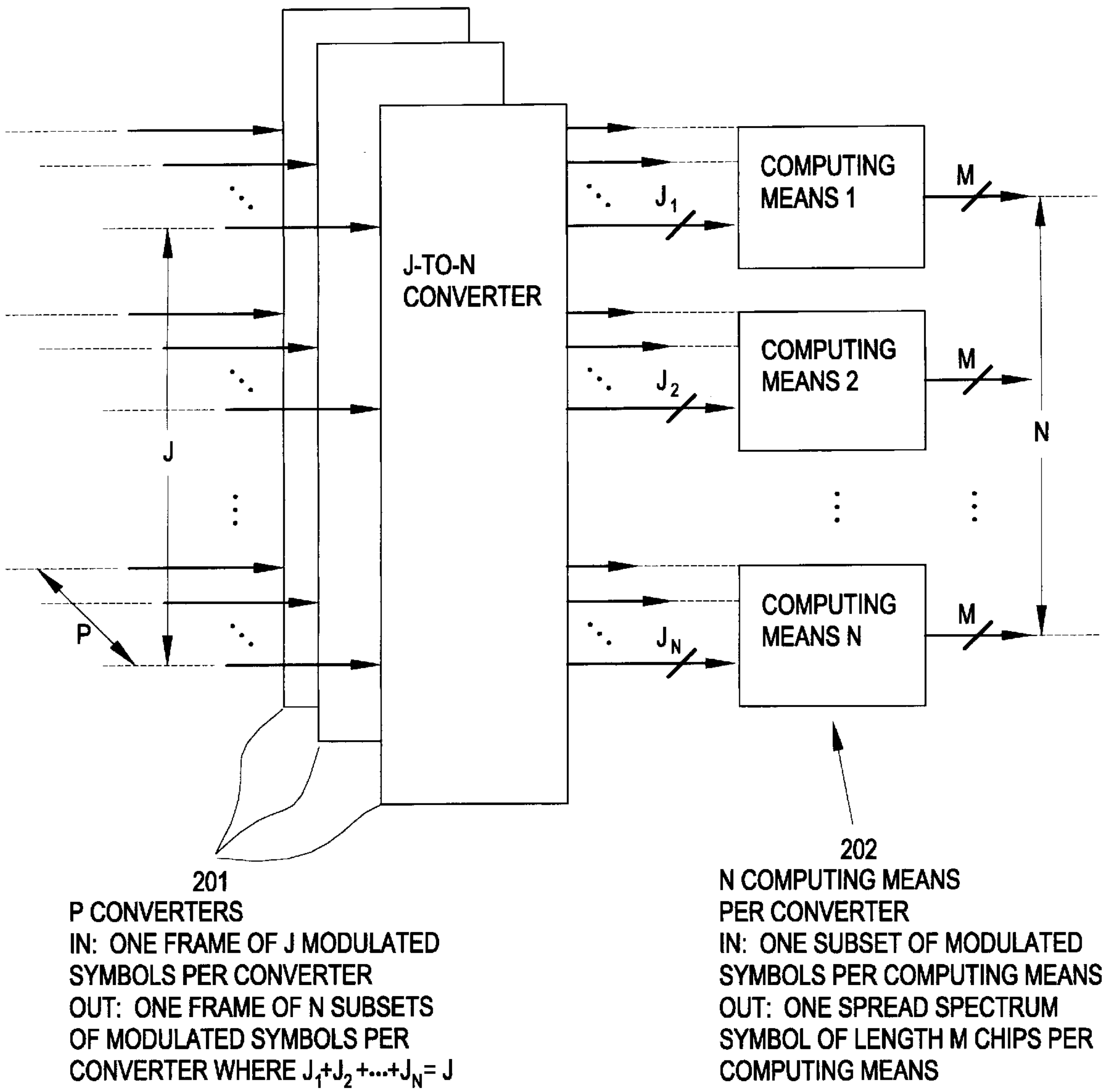

DATA SYMBOLS
SERIAL TO PARALLEL CONNECTOR
B
Q
101
IN: B DATA SYMBOLS
OUT: ONE FRAME OF B DATA SYMBOLS
102
2D SHIFT REGISTER
IN: SHIFTING FROM LEFT TO RIGHT V TIMES
103
CHANNEL ENCODER/MODULATOR
IN: Q FRAMES OF B DATA SYMBOLS EACH
OUT: P FRAMES OF J MODULATED SYMBOLS EACH
104
SPREADER TYPE 1
IN: P FRAMES OF J MODULATED SYMBOLS EACH
OUT: P FRAMES OF N SPREAD SPECTRUM SYMBOLS EACH, OF LENGTH M CHIPS PER SPECTRUM SYMBOL

FIG. 1A

FIG. 1B

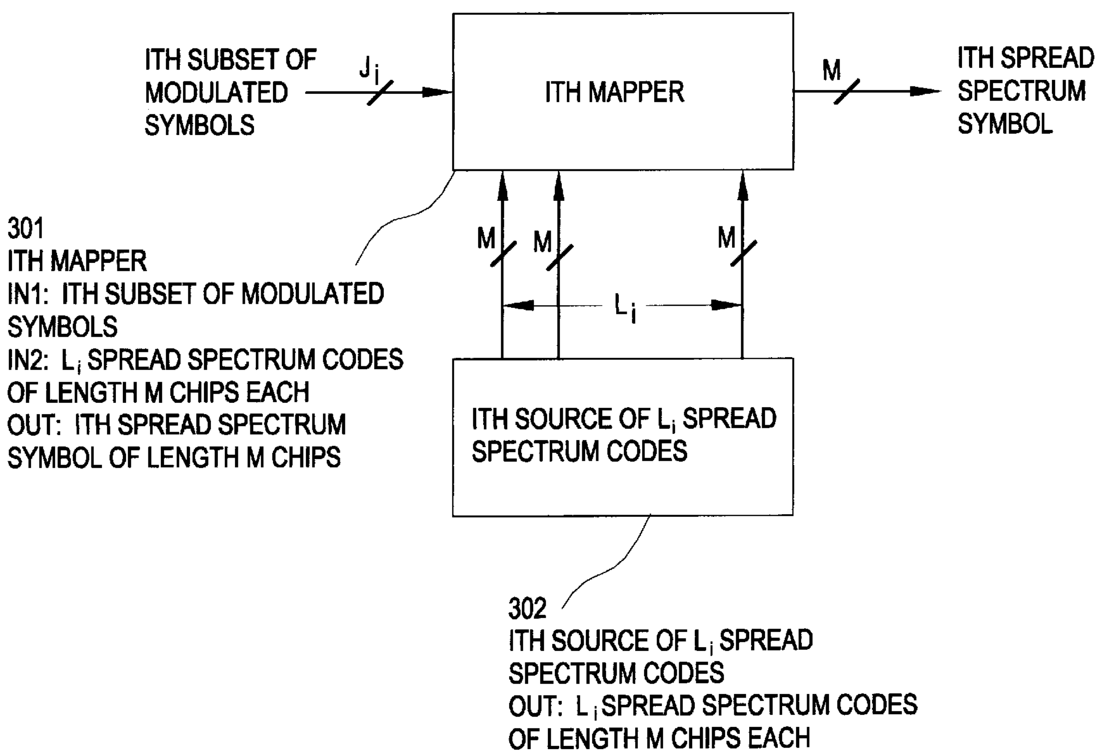

107
IN: ONE FRAME OF M MULTICODED SS SYMBOLS
OUT: M MULTICODED SS SYMBOLS
ADDERS
N
M
P
PARALLEL TO SERIES CONVERTER
MULTICODED SS SYMBOLS
105
3D SHIFT REGISTER
IN: SHIFTING FROM INSIDE TO OUTSIDE M TIMES TO FILL THE SHIFT REGISTER
OUT: SHIFTING FROM LEFT TO RIGHT P TIMES TO EMPTY THE SHIFT REGISTER
106
M ADDERS
IN: N CHIPS PER ADDER
OUT : 1 MULTICODED SS SYMBOL PER ADDER

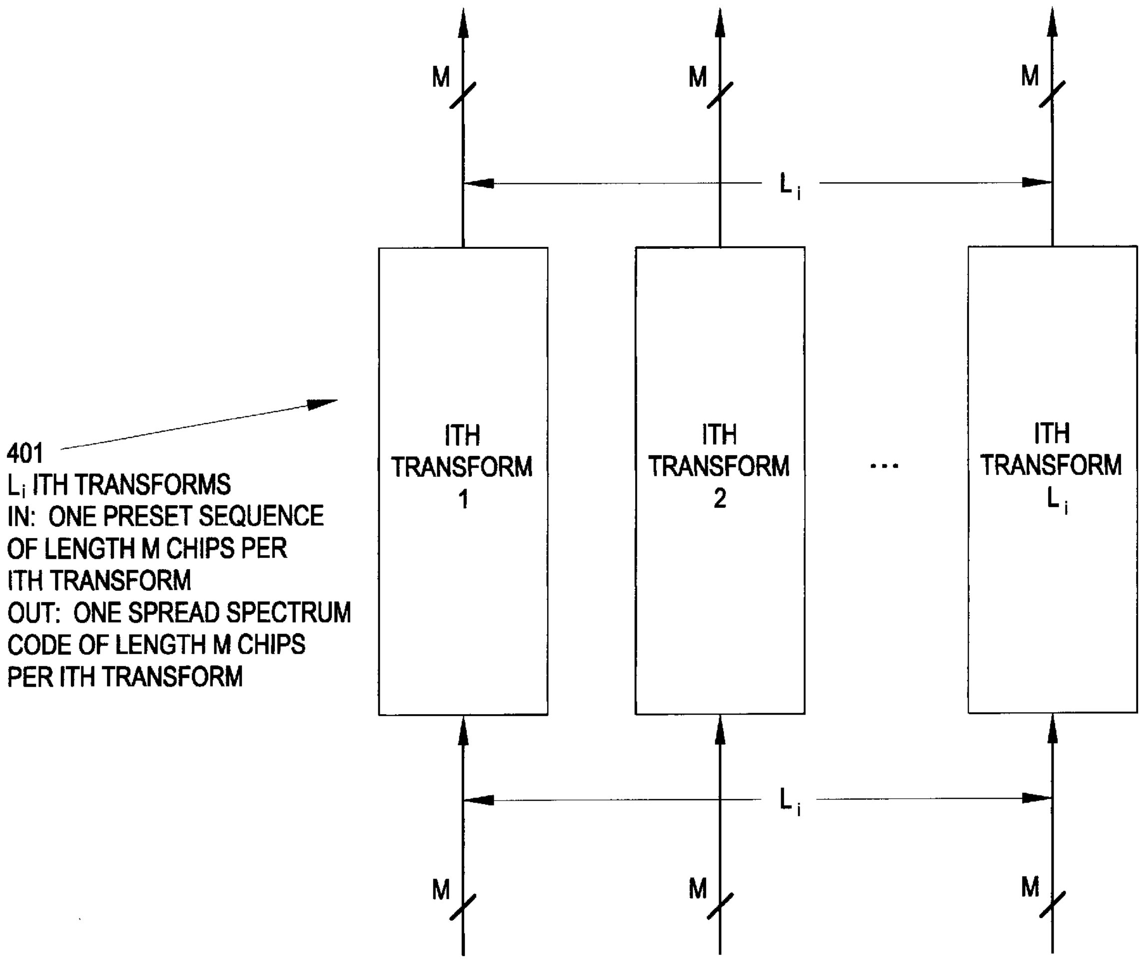


J-TO-N
CONVERTER
COMPUTING
MEANS 1
COMPUTING
MEANS 2
COMPUTING
MEANS N
M
M
M
N
J
P
J_1
J_2
J_N
201
P CONVERTERS
IN: ONE FRAME OF J MODULATED
SYMBOLS PER CONVERTER
OUT: ONE FRAME OF N SUBSETS
OF MODULATED SYMBOLS PER
CONVERTER WHERE $J_1+J_2+\dots+J_N=J$
202
N COMPUTING MEANS
PER CONVERTER
IN: ONE SUBSET OF MODULATED
SYMBOLS PER COMPUTING MEANS
OUT: ONE SPREAD SPECTRUM
SYMBOL OF LENGTH M CHIPS PER
COMPUTING MEANS

FIG. 2

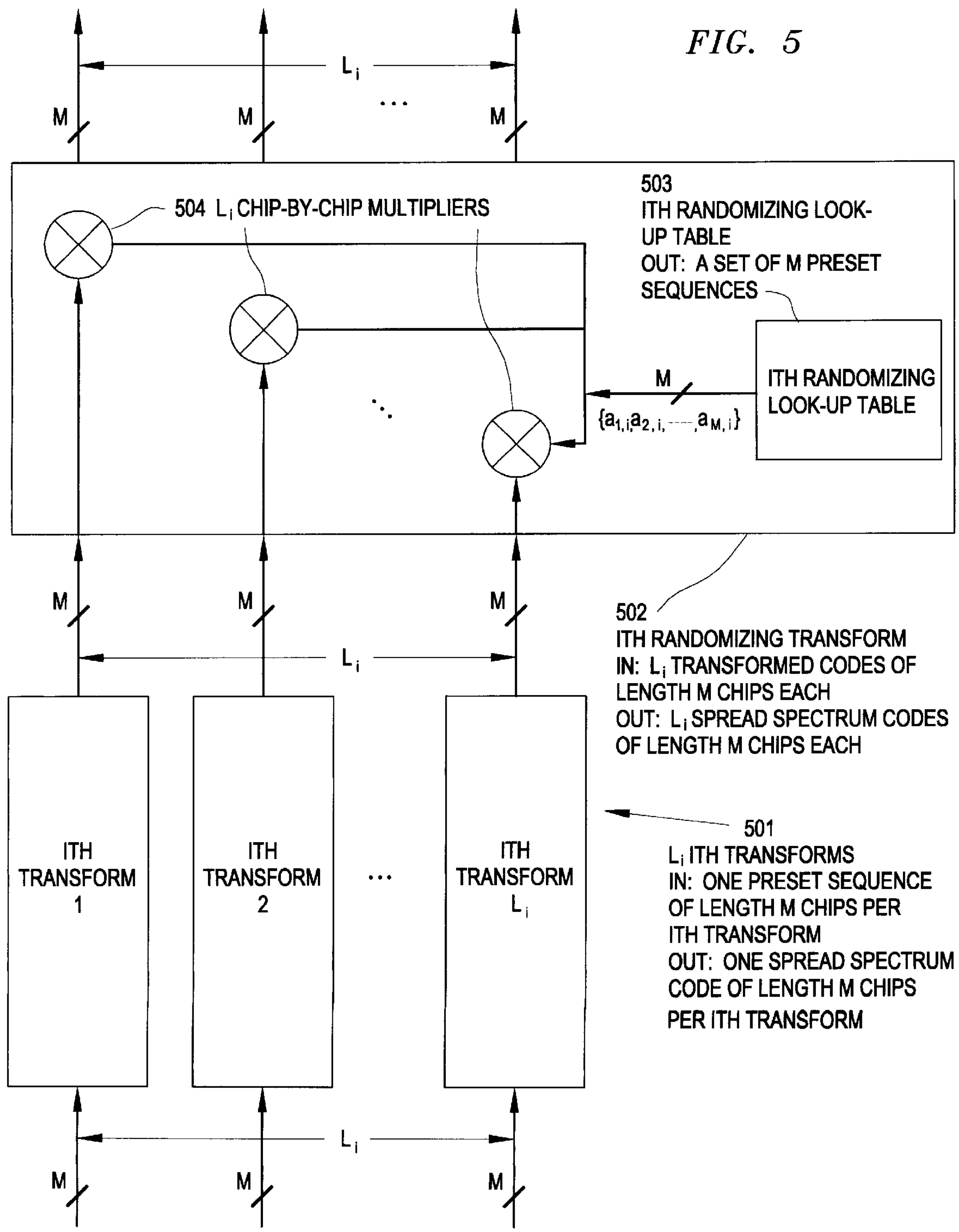
FIG. 3


ITH SUBSET OF MODULATED SYMBOLS
J_i
ITH MAPPER
M
ITH SPREAD SPECTRUM SYMBOL
301
ITH MAPPER
IN1: ITH SUBSET OF MODULATED SYMBOLS
IN2: L_i SPREAD SPECTRUM CODES OF LENGTH M CHIPS EACH
OUT: ITH SPREAD SPECTRUM SYMBOL OF LENGTH M CHIPS
M
M
M
L_i
ITH SOURCE OF L_i SPREAD SPECTRUM CODES
302
ITH SOURCE OF L_i SPREAD SPECTRUM CODES
OUT: L_i SPREAD SPECTRUM CODES OF LENGTH M CHIPS EACH



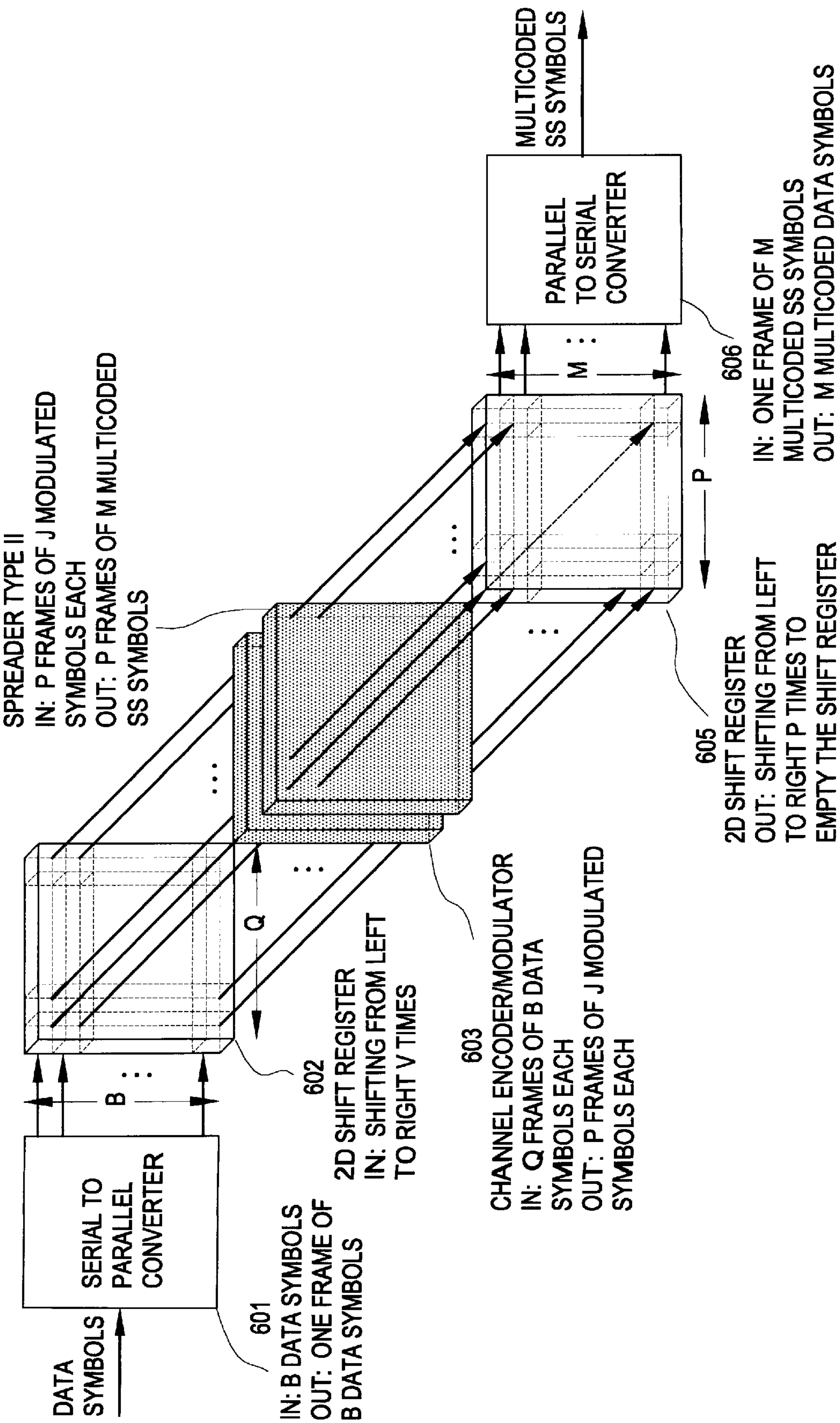
401
L_i ITH TRANSFORMS
IN: ONE PRESET SEQUENCE OF LENGTH M CHIPS PER ITH TRANSFORM
OUT: ONE SPREAD SPECTRUM CODE OF LENGTH M CHIPS PER ITH TRANSFORM
ITH TRANSFORM 1
ITH TRANSFORM 2
...
ITH TRANSFORM L_i
M
M
M
L_i
L_i
M
M
M

FIG. 4



L_i
M
M
M
504 L_i CHIP-BY-CHIP MULTIPLIERS
503
ITH RANDOMIZING LOOK-UP TABLE
OUT: A SET OF M PRESET SEQUENCES
M
ITH RANDOMIZING LOOK-UP TABLE
$\{a_{1,i}, a_{2,i}, ---, a_{M,i}\}$
M
M
M
L_i
502
ITH RANDOMIZING TRANSFORM
IN: L_i TRANSFORMED CODES OF LENGTH M CHIPS EACH
OUT: L_i SPREAD SPECTRUM CODES OF LENGTH M CHIPS EACH
ITH TRANSFORM 1
ITH TRANSFORM 2
ITH TRANSFORM L_i
501
L_i ITH TRANSFORMS
IN: ONE PRESET SEQUENCE OF LENGTH M CHIPS PER ITH TRANSFORM
OUT: ONE SPREAD SPECTRUM CODE OF LENGTH M CHIPS PER ITH TRANSFORM
L_i
M
M
M

FIG. 5



DATA SYMBOLS
SERIAL TO PARALLEL CONVERTER
601
IN: B DATA SYMBOLS
OUT: ONE FRAME OF B DATA SYMBOLS
B
Q
602
2D SHIFT REGISTER
IN: SHIFTING FROM LEFT TO RIGHT V TIMES
603
CHANNEL ENCODER/MODULATOR
IN: Q FRAMES OF B DATA SYMBOLS EACH
OUT: P FRAMES OF J MODULATED SYMBOLS EACH
604
SPREADER TYPE II
IN: P FRAMES OF J MODULATED SYMBOLS EACH
OUT: P FRAMES OF M MULTICODED SS SYMBOLS
605
2D SHIFT REGISTER
OUT: SHIFTING FROM LEFT TO RIGHT P TIMES TO EMPTY THE SHIFT REGISTER
P
M
PARALLEL TO SERIAL CONVERTER
606
IN: ONE FRAME OF M MULTICODED SS SYMBOLS
OUT: M MULTICODED DATA SYMBOLS
MULTICODED SS SYMBOLS

FIG. 6

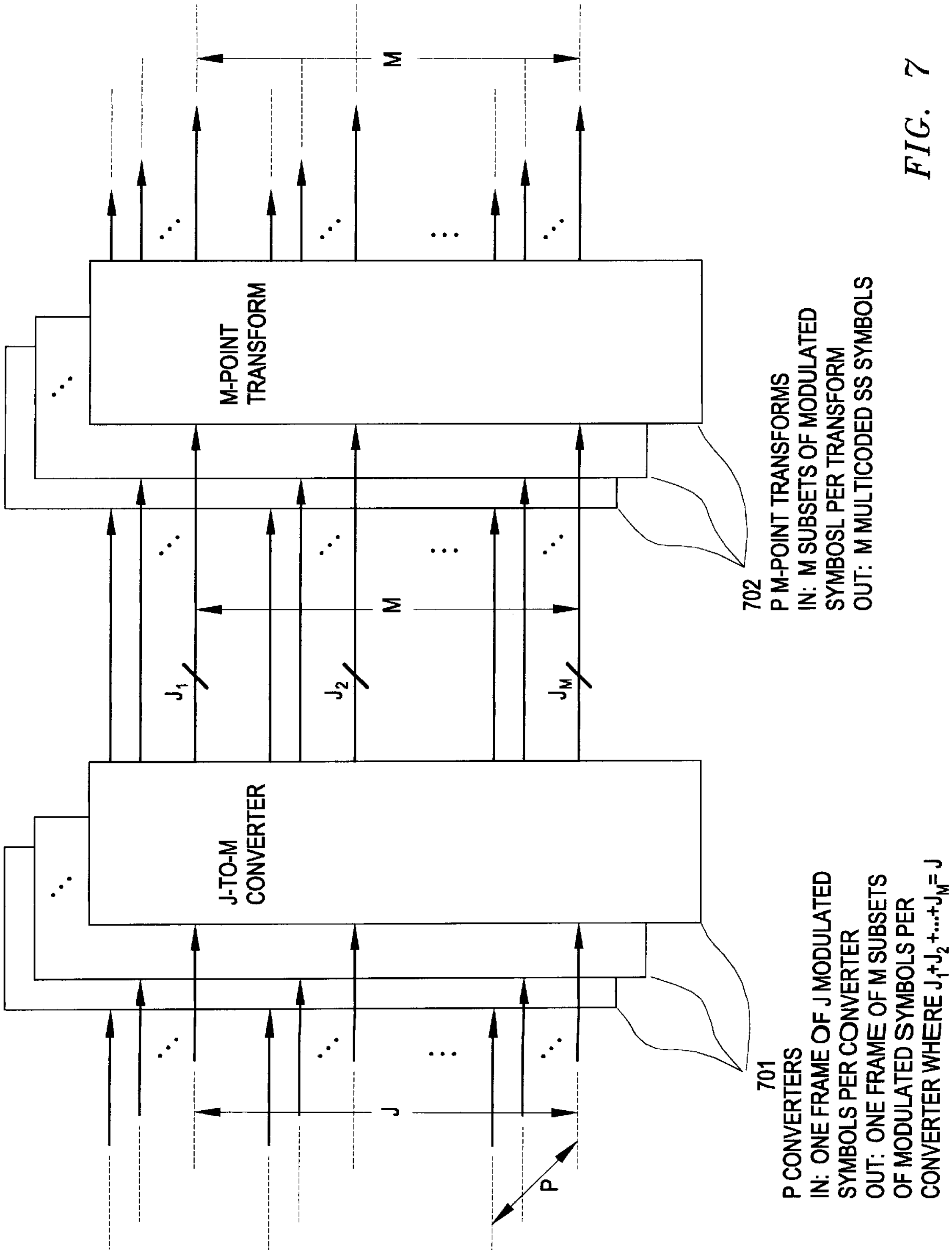
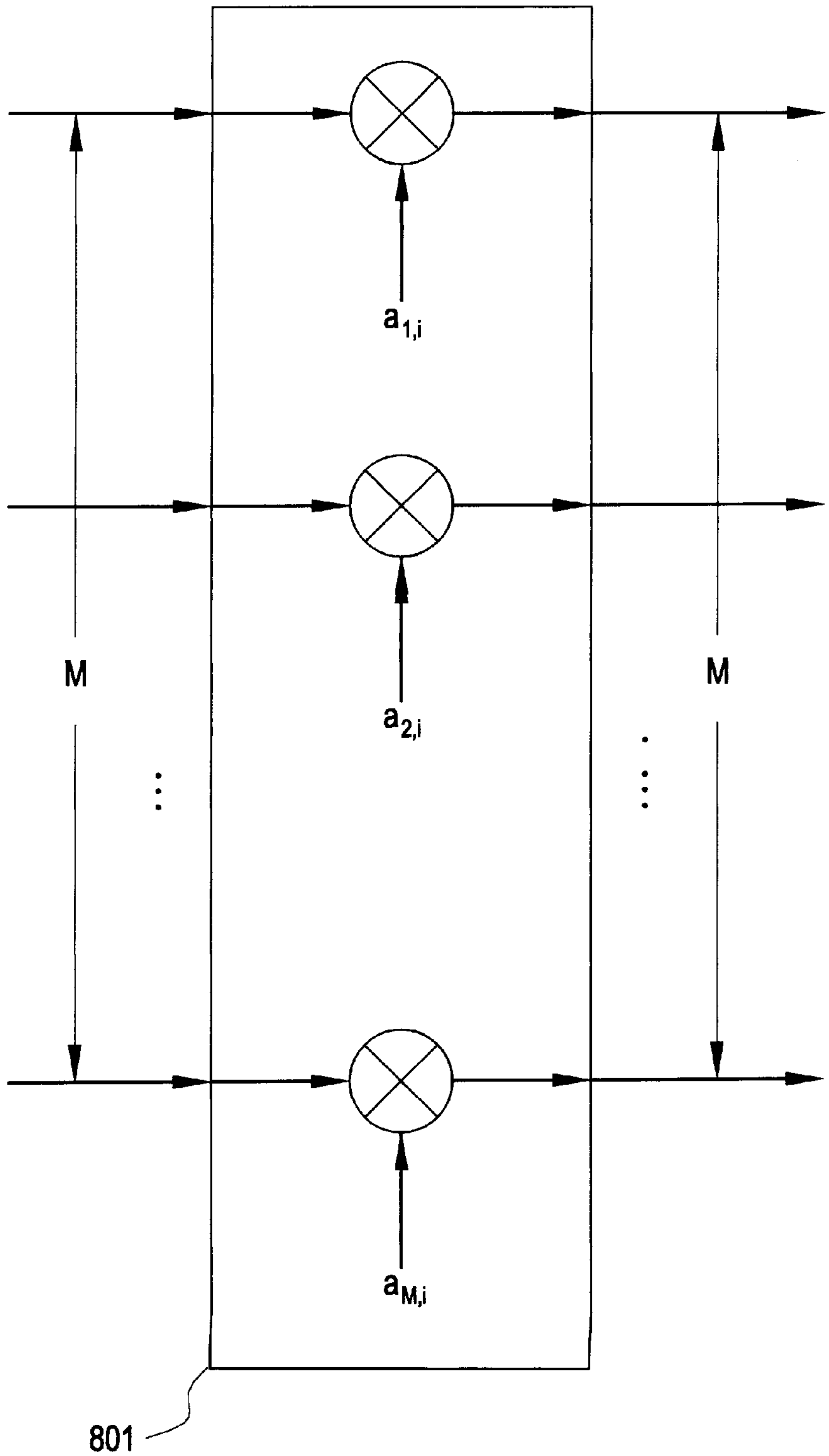

M-POINT TRANSFORM
J-TO-M CONVERTER
M
M
J
P
J_1
J_2
J_M
702
P M-POINT TRANSFORMS
IN: M SUBSETS OF MODULATED SYMBOSL PER TRANSFORM
OUT: M MULTICODED SS SYMBOLS
701
P CONVERTERS
IN: ONE FRAME OF J MODULATED SYMBOLS PER CONVERTER
OUT: ONE FRAME OF M SUBSETS OF MODULATED SYMBOLS PER CONVERTER WHERE $J_1+J_2+...+J_M=J$

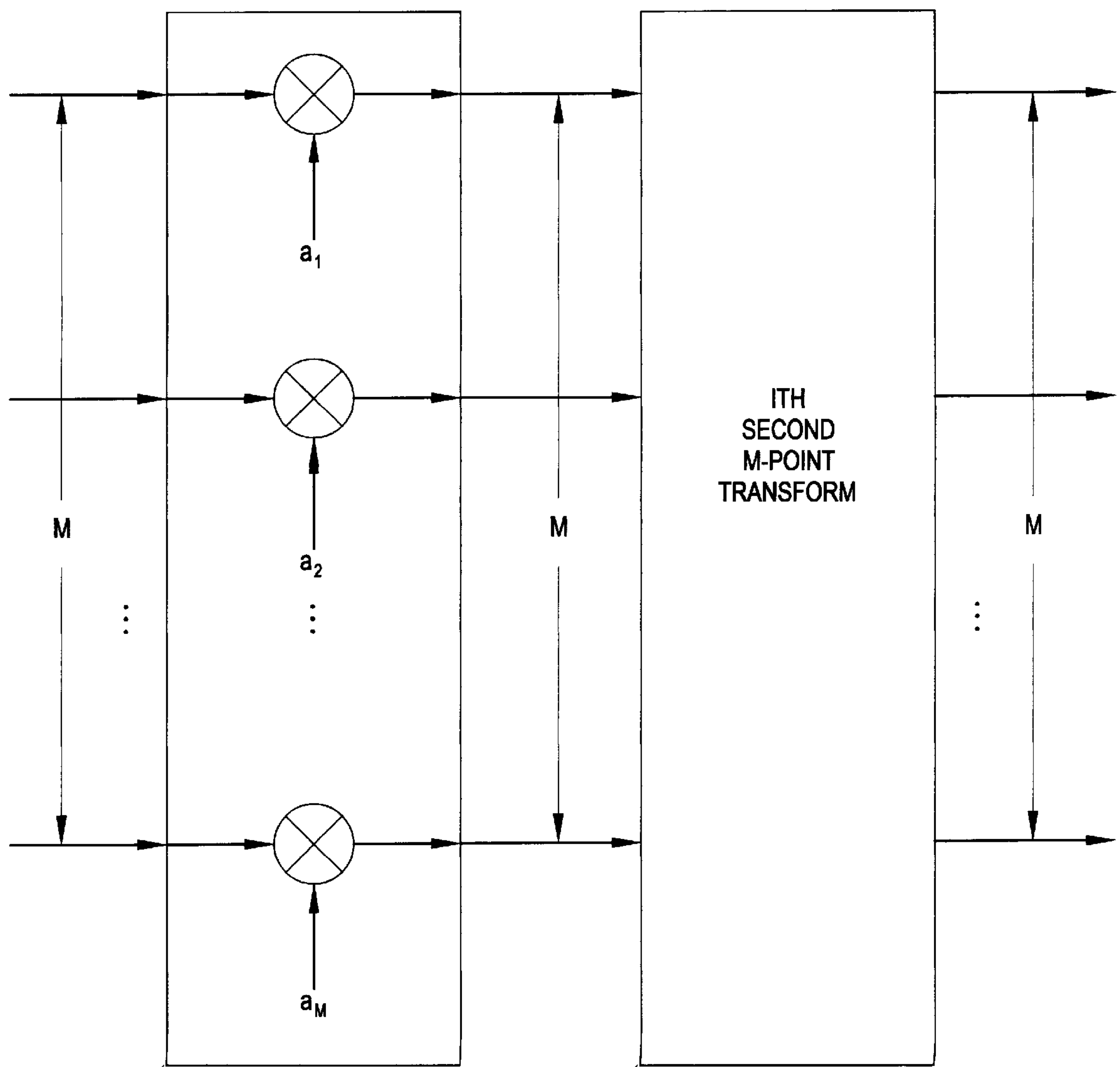
FIG. 7

FIG. 8



ITH M-POINT RANDOMIZING TRANSFORM
IN: M SUBSETS OF MODULATED SYMBOLS
OUT: M MULTICODED SS SYMBOLS

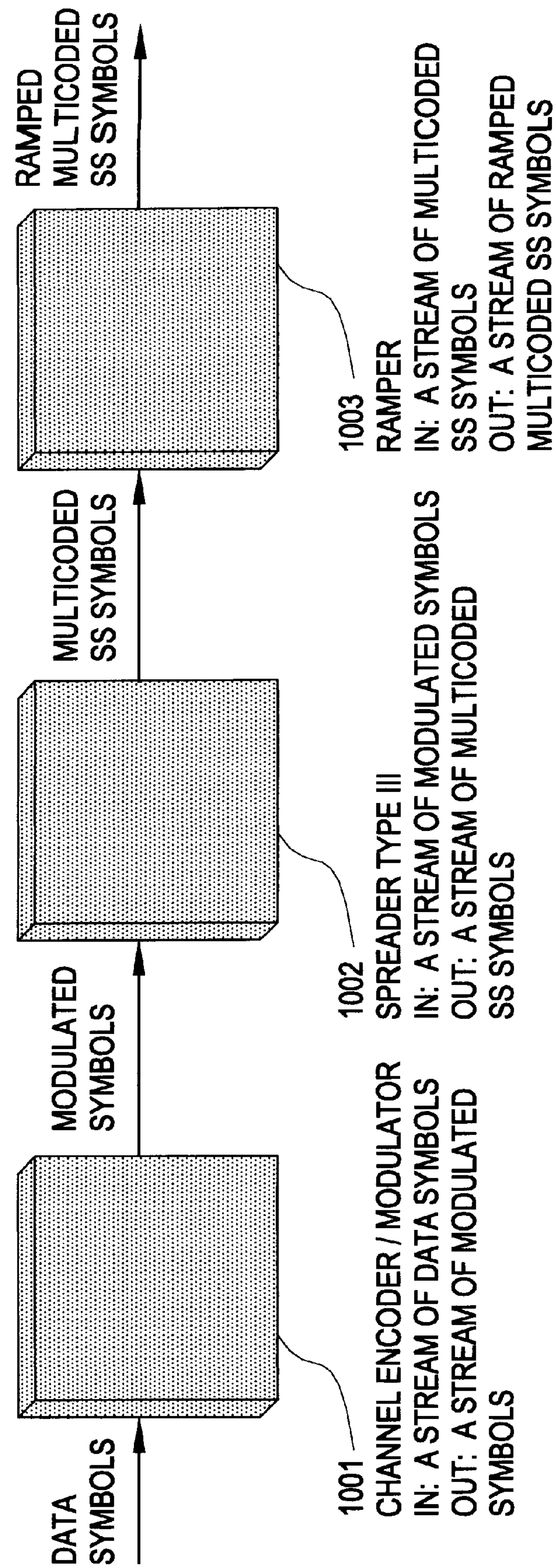
FIG. 9



901
ITH M-POINT RANDOMIZING TRANSFORM
IN: M SUBSETS OF MODULATED SYMBOLS
OUT: M TRANSFORMED SYMBOLS

902
ITH SECOND M-POINT TRANSFORM
IN: M TRANSFORMED SYMBOLS
OUT: M MULTICODED SS SYMBOLS

FIG. 10


DATA SYMBOLS
MODULATED SYMBOLS
MULTICODED SS SYMBOLS
RAMPED MULTICODED SS SYMBOLS
1001
CHANNEL ENCODER / MODULATOR
IN: A STREAM OF DATA SYMBOLS
OUT: A STREAM OF MODULATED SYMBOLS
1002
SPREADER TYPE III
IN: A STREAM OF MODULATED SYMBOLS
OUT: A STREAM OF MULTICODED SS SYMBOLS
1003
RAMPER
IN: A STREAM OF MULTICODED SS SYMBOLS
OUT: A STREAM OF RAMPED MULTICODED SS SYMBOLS

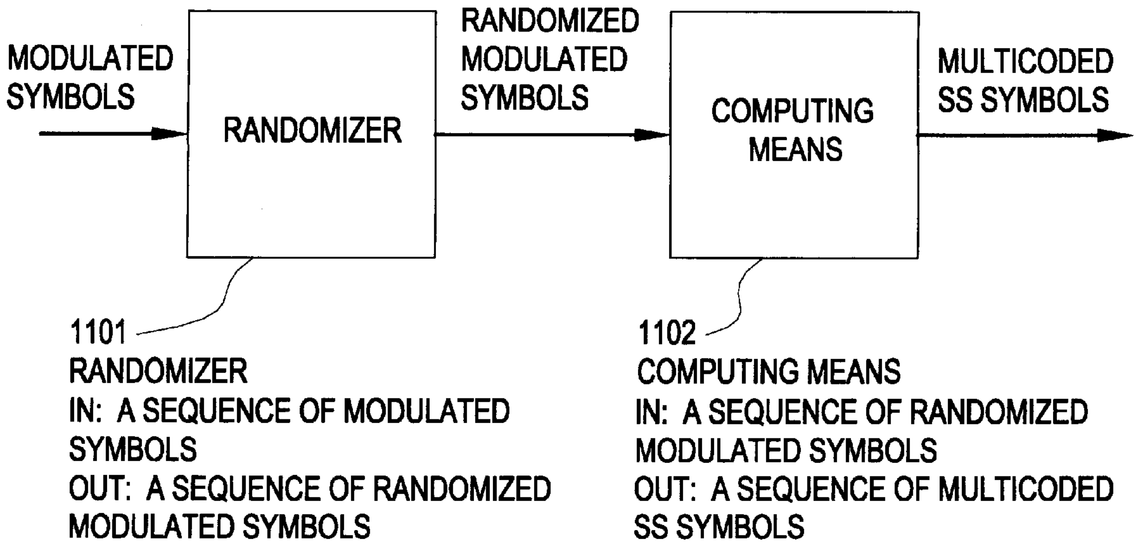

MODULATED
SYMBOLS
RANDOMIZER
RANDOMIZED
MODULATED
SYMBOLS
COMPUTING
MEANS
MULTICODED
SS SYMBOLS
1101
RANDOMIZER
IN: A SEQUENCE OF MODULATED
SYMBOLS
OUT: A SEQUENCE OF RANDOMIZED
MODULATED SYMBOLS
1102
COMPUTING MEANS
IN: A SEQUENCE OF RANDOMIZED
MODULATED SYMBOLS
OUT: A SEQUENCE OF MULTICODED
SS SYMBOLS

FIG. 11

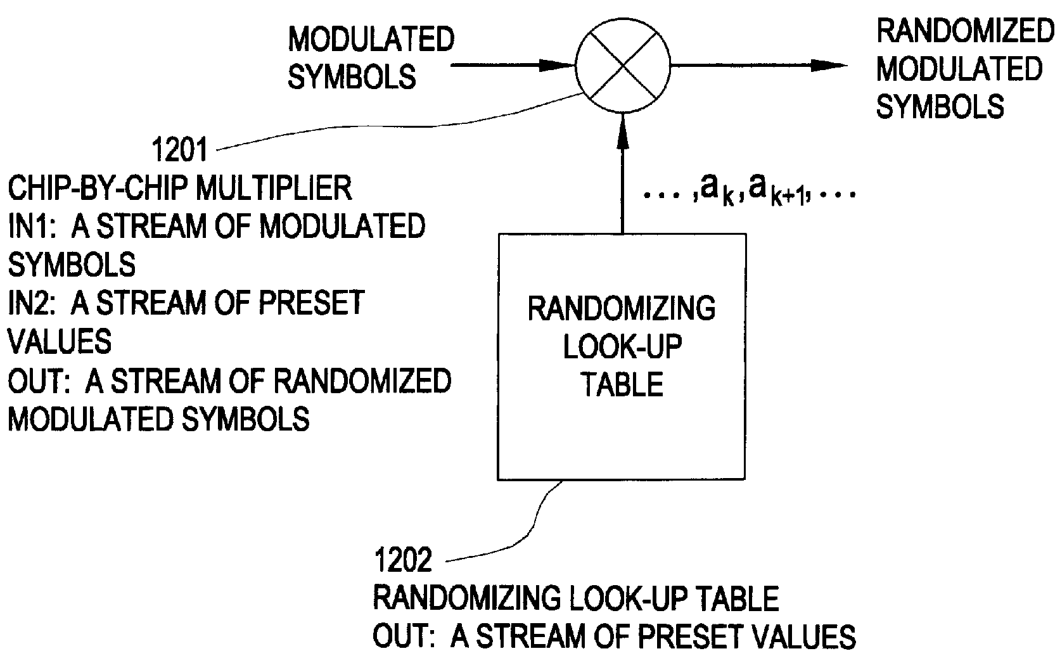

MODULATED
SYMBOLS
RANDOMIZED
MODULATED
SYMBOLS
1201
CHIP-BY-CHIP MULTIPLIER
IN1: A STREAM OF MODULATED
SYMBOLS
IN2: A STREAM OF PRESET
VALUES
OUT: A STREAM OF RANDOMIZED
MODULATED SYMBOLS
. . . ,a_k,a_{k+1}, . . .
RANDOMIZING
LOOK-UP
TABLE
1202
RANDOMIZING LOOK-UP TABLE
OUT: A STREAM OF PRESET VALUES

FIG. 12

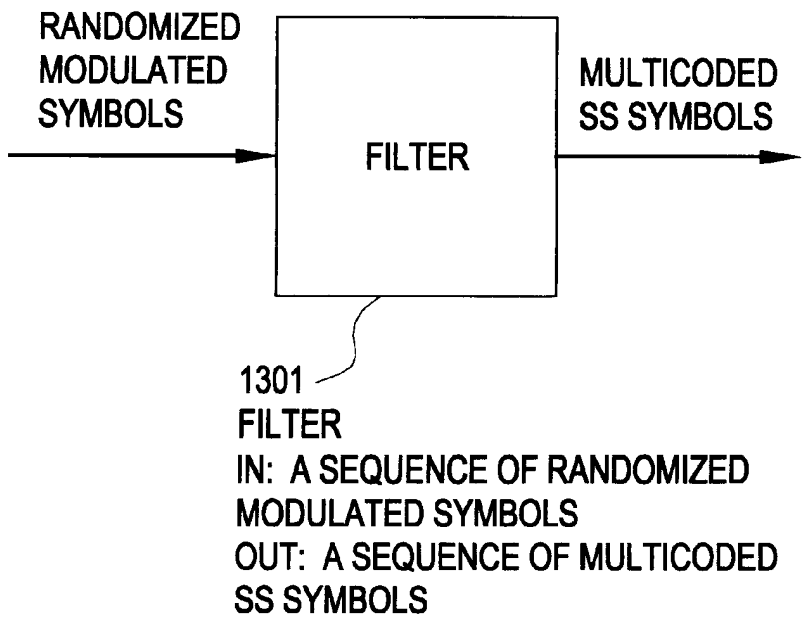

RANDOMIZED
MODULATED
SYMBOLS
FILTER
MULTICODED
SS SYMBOLS
1301
FILTER
IN: A SEQUENCE OF RANDOMIZED
MODULATED SYMBOLS
OUT: A SEQUENCE OF MULTICODED
SS SYMBOLS

FIG. 13

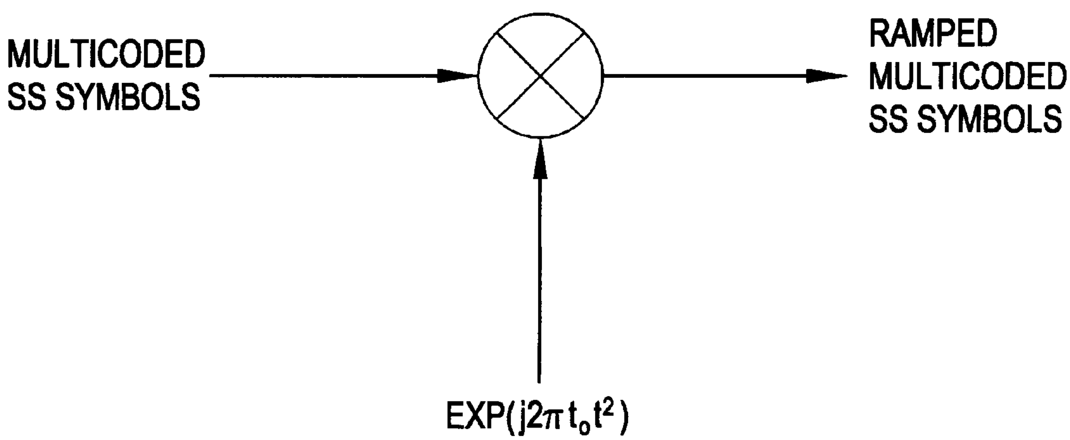

MULTICODED
SS SYMBOLS
RAMPED
MULTICODED
SS SYMBOLS
EXP($j2\pi t_o t^2$)

FIG. 14

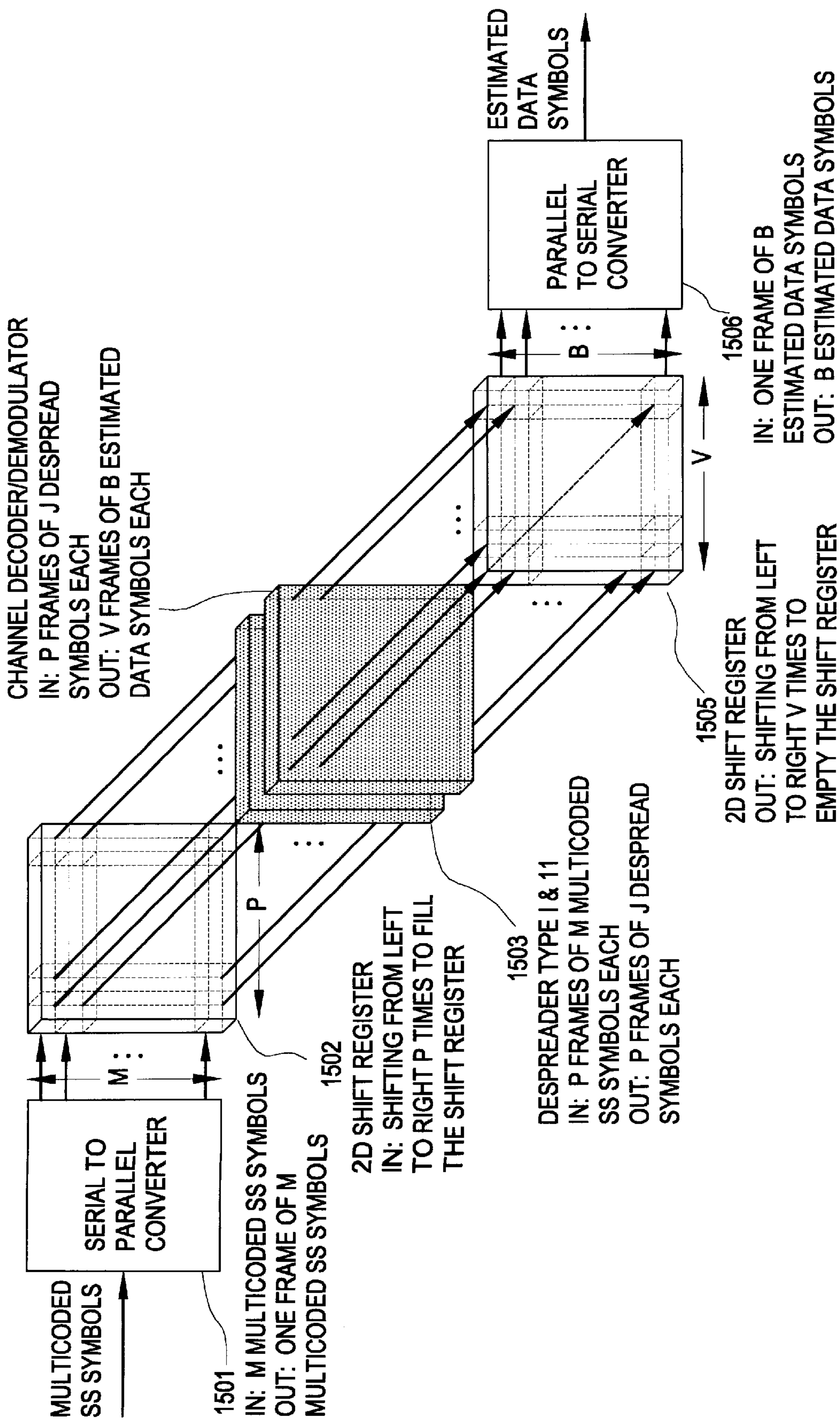

MULTICODED SS SYMBOLS
SERIAL TO PARALLEL CONVERTER
1501
IN: M MULTICODED SS SYMBOLS
OUT: ONE FRAME OF M MULTICODED SS SYMBOLS
M
P
1502
2D SHIFT REGISTER
IN: SHIFTING FROM LEFT TO RIGHT P TIMES TO FILL THE SHIFT REGISTER
1503
DESPREADER TYPE I & II
IN: P FRAMES OF M MULTICODED SS SYMBOLS EACH
OUT: P FRAMES OF J DESPREAD SYMBOLS EACH
1504
CHANNEL DECODER/DEMODULATOR
IN: P FRAMES OF J DESPREAD SYMBOLS EACH
OUT: V FRAMES OF B ESTIMATED DATA SYMBOLS EACH
V
1505
2D SHIFT REGISTER
OUT: SHIFTING FROM LEFT TO RIGHT V TIMES TO EMPTY THE SHIFT REGISTER
B
PARALLEL TO SERIAL CONVERTER
1506
IN: ONE FRAME OF B ESTIMATED DATA SYMBOLS
OUT: B ESTIMATED DATA SYMBOLS
ESTIMATED DATA SYMBOLS

FIG. 15

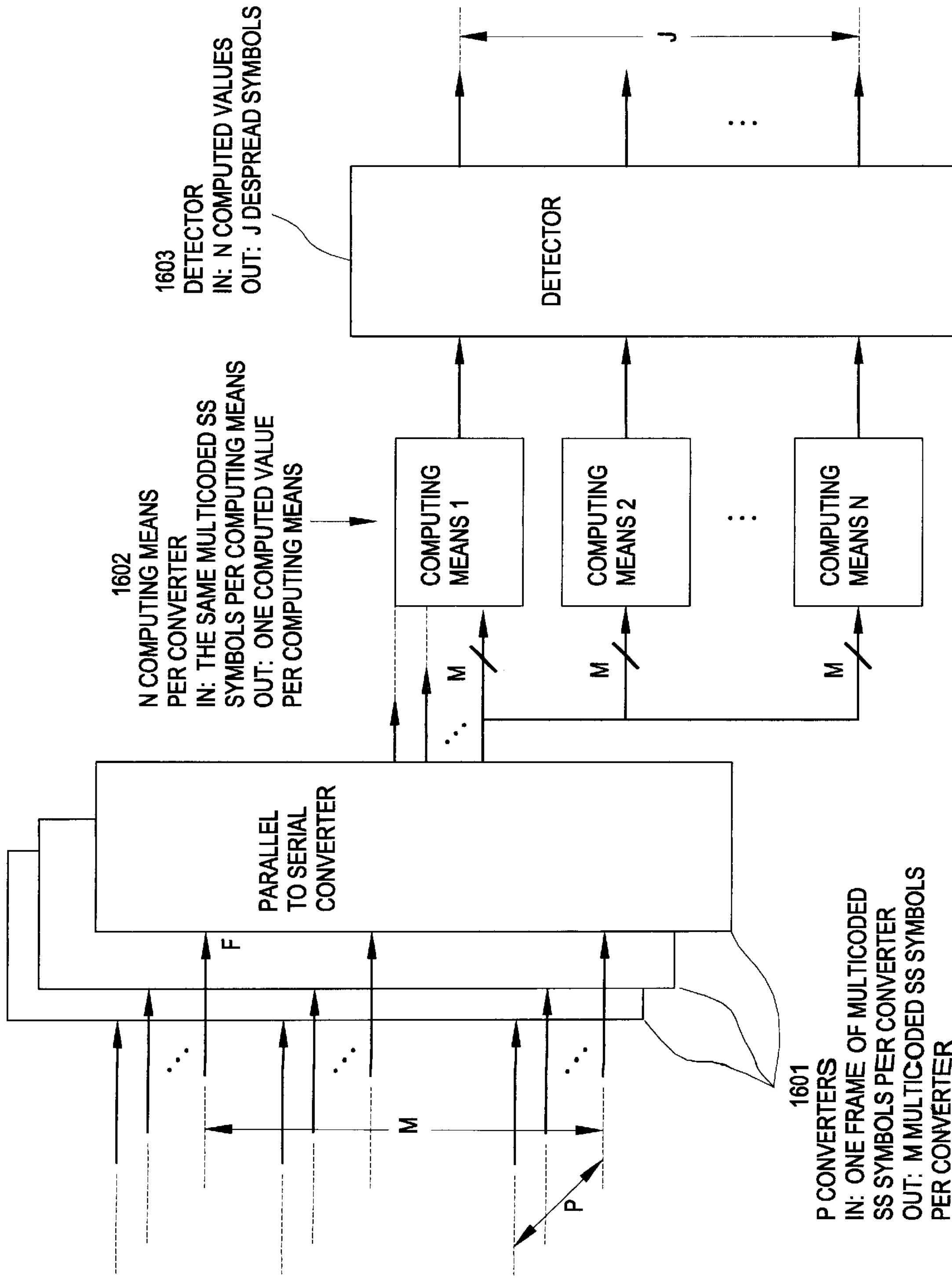
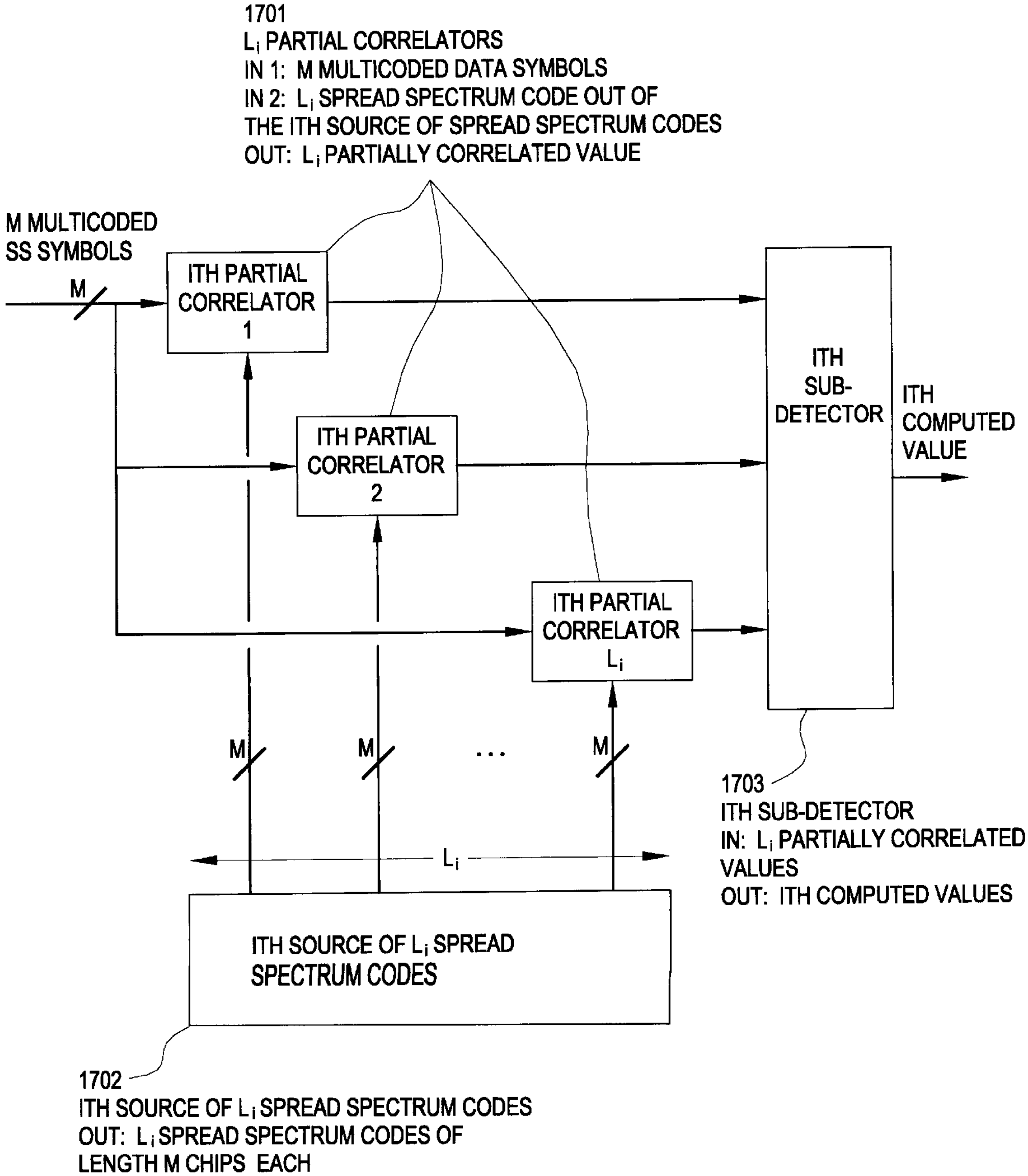

1603
DETECTOR
IN: N COMPUTED VALUES
OUT: J DESPREAD SYMBOLS
DETECTOR
J
1602
N COMPUTING MEANS
PER CONVERTER
IN: THE SAME MULTICODED SS
SYMBOLS PER COMPUTING MEANS
OUT: ONE COMPUTED VALUE
PER COMPUTING MEANS
COMPUTING MEANS 1
COMPUTING MEANS 2
COMPUTING MEANS N
M
M
M
PARALLEL
TO SERIAL
CONVERTER
F
M
P
1601
P CONVERTERS
IN: ONE FRAME OF MULTICODED
SS SYMBOLS PER CONVERTER
OUT: M MULTICODED SS SYMBOLS
PER CONVERTER

FIG. 16

FIG. 17


1701
L_i PARTIAL CORRELATORS
IN 1: M MULTICODED DATA SYMBOLS
IN 2: L_i SPREAD SPECTRUM CODE OUT OF
THE ITH SOURCE OF SPREAD SPECTRUM CODES
OUT: L_i PARTIALLY CORRELATED VALUE
M MULTICODED
SS SYMBOLS
M
ITH PARTIAL
CORRELATOR
1
ITH PARTIAL
CORRELATOR
2
ITH PARTIAL
CORRELATOR
L_i
ITH
SUB-
DETECTOR
ITH
COMPUTED
VALUE
M
M
. . .
M
L_i
ITH SOURCE OF L_i SPREAD
SPECTRUM CODES
1703
ITH SUB-DETECTOR
IN: L_i PARTIALLY CORRELATED
VALUES
OUT: ITH COMPUTED VALUES
1702
ITH SOURCE OF L_i SPREAD SPECTRUM CODES
OUT: L_i SPREAD SPECTRUM CODES OF
LENGTH M CHIPS EACH

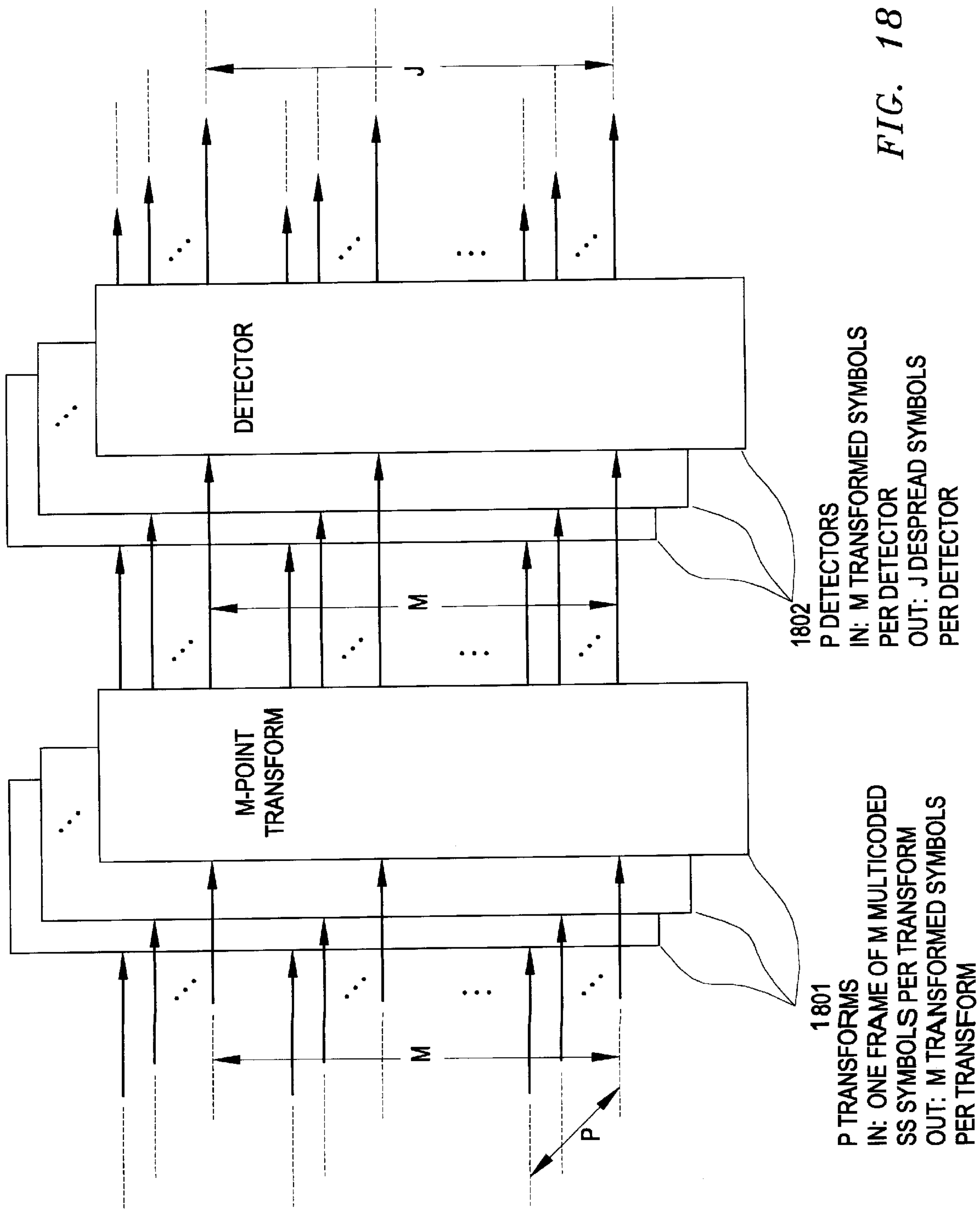

M-POINT TRANSFORM
DETECTOR
M
M
J
P
1801
P TRANSFORMS
IN: ONE FRAME OF M MULTICODED SS SYMBOLS PER TRANSFORM
OUT: M TRANSFORMED SYMBOLS PER TRANSFORM
1802
P DETECTORS
IN: M TRANSFORMED SYMBOLS PER DETECTOR
OUT: J DESPREAD SYMBOLS PER DETECTOR

FIG. 18

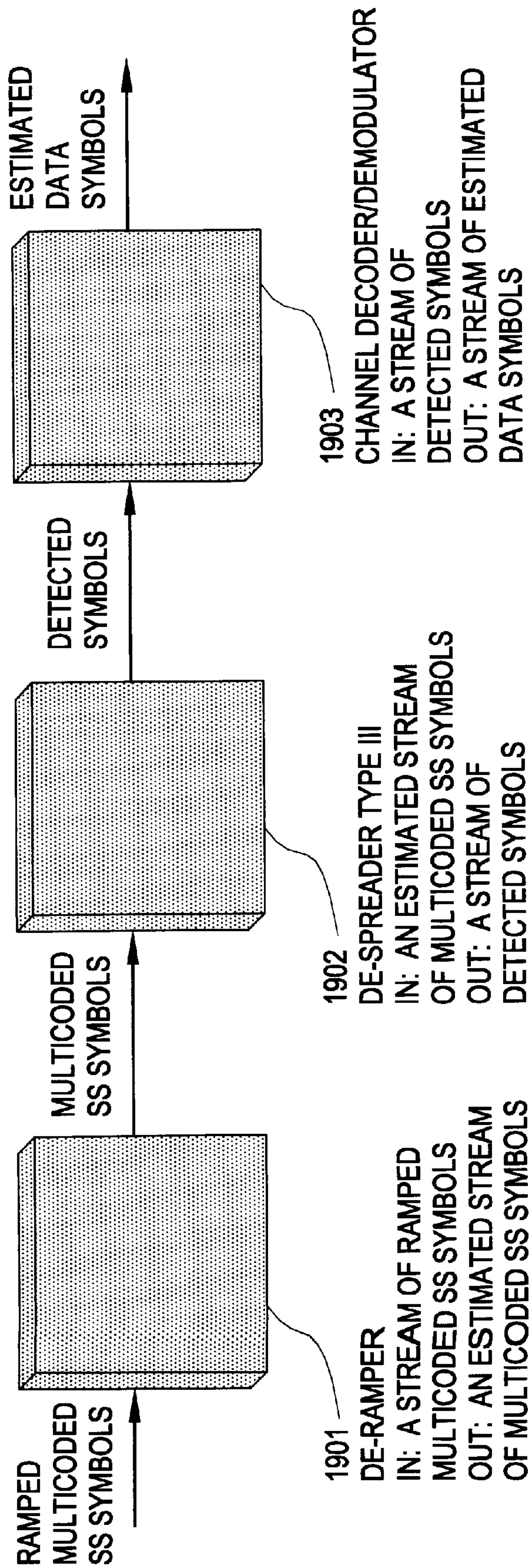

RAMPED MULTICODED SS SYMBOLS
1901
DE-RAMPER
IN: A STREAM OF RAMPED MULTICODED SS SYMBOLS
OUT: AN ESTIMATED STREAM OF MULTICODED SS SYMBOLS
MULTICODED SS SYMBOLS
1902
DE-SPREADER TYPE III
IN: AN ESTIMATED STREAM OF MULTICODED SS SYMBOLS
OUT: A STREAM OF DETECTED SYMBOLS
DETECTED SYMBOLS
1903
CHANNEL DECODER/DEMODULATOR
IN: A STREAM OF DETECTED SYMBOLS
OUT: A STREAM OF ESTIMATED DATA SYMBOLS
ESTIMATED DATA SYMBOLS

FIG. 19

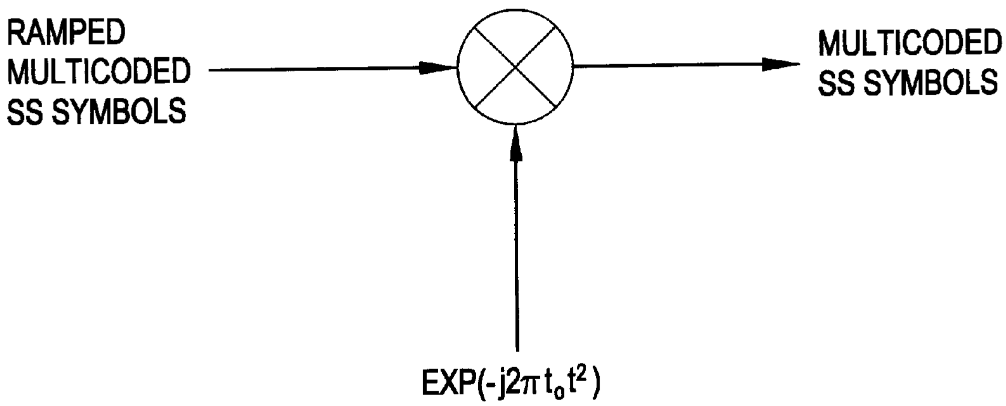

RAMPED
MULTICODED
SS SYMBOLS
MULTICODED
SS SYMBOLS
EXP(-j2π t$_o$t^2)

FIG. 20

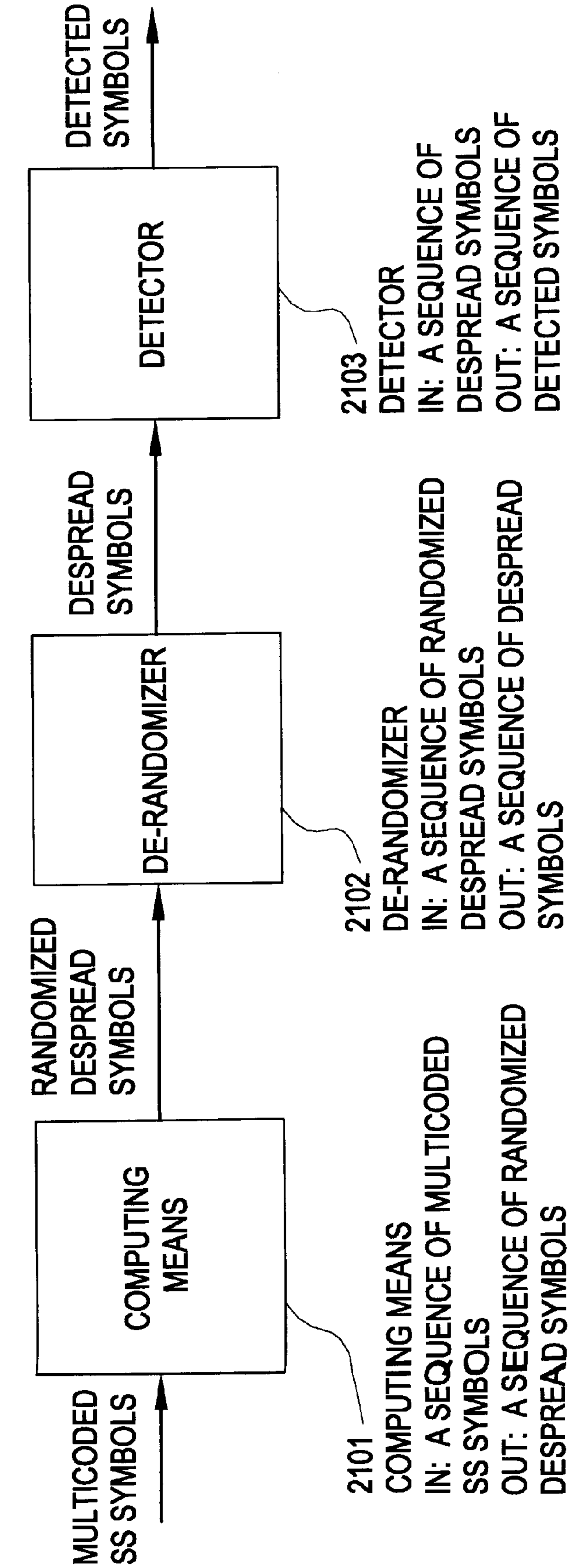

MULTICODED SS SYMBOLS
COMPUTING MEANS
RANDOMIZED DESPREAD SYMBOLS
DE-RANDOMIZER
DESPREAD SYMBOLS
DETECTOR
DETECTED SYMBOLS
2101
COMPUTING MEANS
IN: A SEQUENCE OF MULTICODED SS SYMBOLS
OUT: A SEQUENCE OF RANDOMIZED DESPREAD SYMBOLS
2102
DE-RANDOMIZER
IN: A SEQUENCE OF RANDOMIZED DESPREAD SYMBOLS
OUT: A SEQUENCE OF DESPREAD SYMBOLS
2103
DETECTOR
IN: A SEQUENCE OF DESPREAD SYMBOLS
OUT: A SEQUENCE OF DETECTED SYMBOLS

FIG. 21

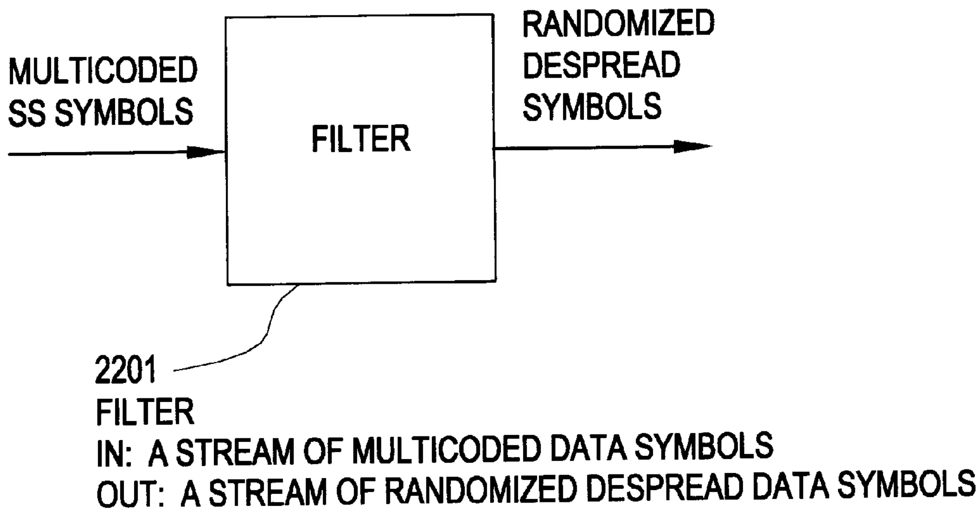

MULTICODED SS SYMBOLS
FILTER
RANDOMIZED DESPREAD SYMBOLS
2201
FILTER
IN: A STREAM OF MULTICODED DATA SYMBOLS
OUT: A STREAM OF RANDOMIZED DESPREAD DATA SYMBOLS

FIG. 22

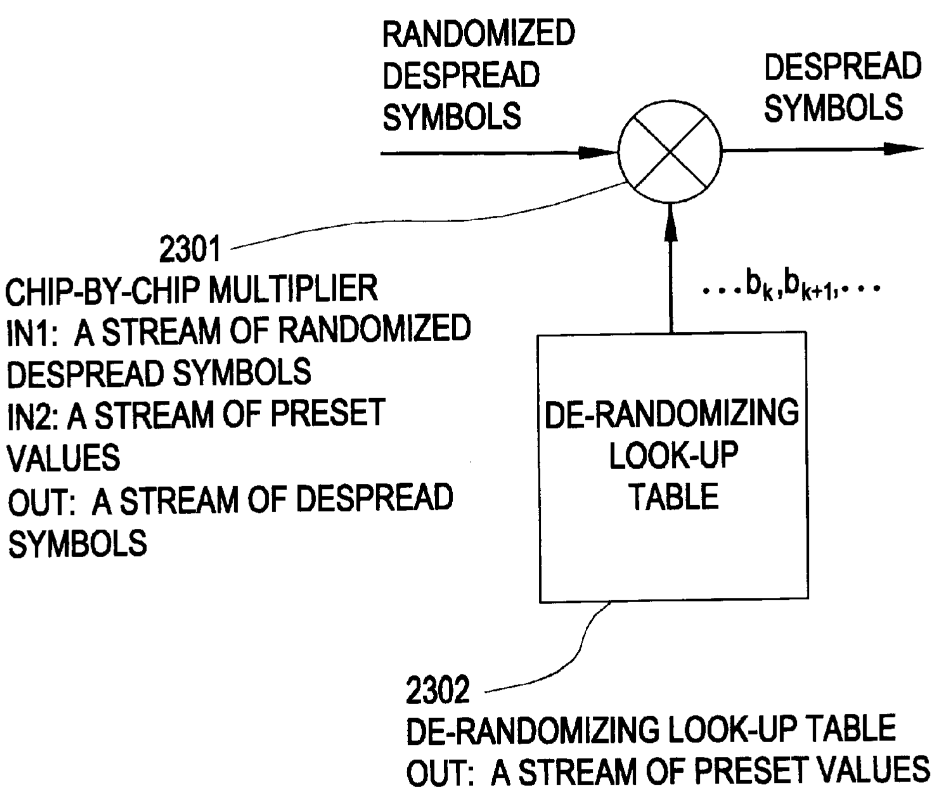

RANDOMIZED DESPREAD SYMBOLS
DESPREAD SYMBOLS
2301
CHIP-BY-CHIP MULTIPLIER
IN1: A STREAM OF RANDOMIZED DESPREAD SYMBOLS
IN2: A STREAM OF PRESET VALUES
OUT: A STREAM OF DESPREAD SYMBOLS
...b_k,b_{k+1},...
DE-RANDOMIZING LOOK-UP TABLE
2302
DE-RANDOMIZING LOOK-UP TABLE
OUT: A STREAM OF PRESET VALUES

FIG. 23

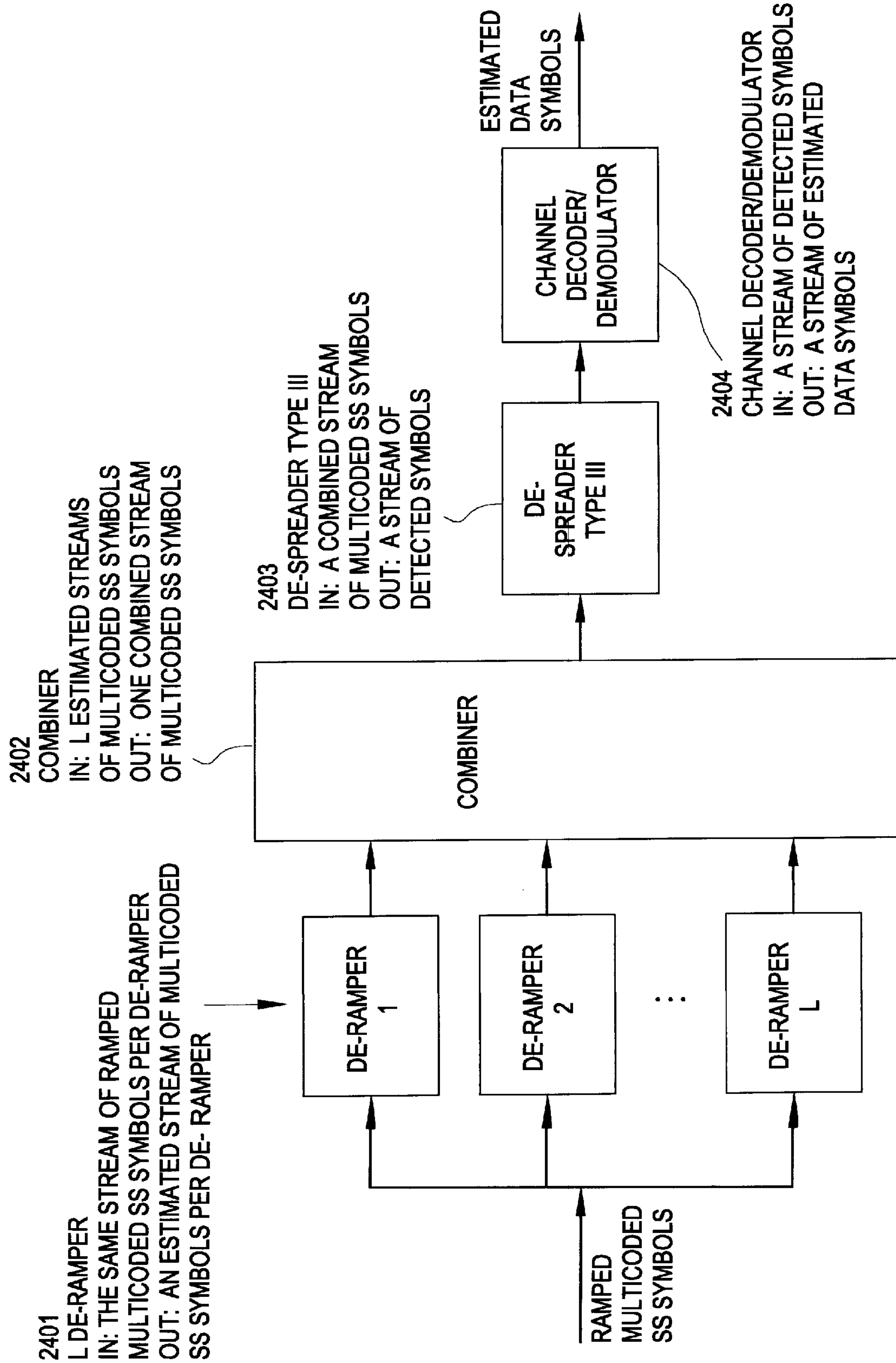

2401
L DE-RAMPER
IN: THE SAME STREAM OF RAMPED MULTICODED SS SYMBOLS PER DE-RAMPER
OUT: AN ESTIMATED STREAM OF MULTICODED SS SYMBOLS PER DE- RAMPER
RAMPED MULTICODED SS SYMBOLS
DE-RAMPER 1
DE-RAMPER 2
...
DE-RAMPER L
2402
COMBINER
IN: L ESTIMATED STREAMS OF MULTICODED SS SYMBOLS
OUT: ONE COMBINED STREAM OF MULTICODED SS SYMBOLS
COMBINER
2403
DE-SPREADER TYPE III
IN: A COMBINED STREAM OF MULTICODED SS SYMBOLS
OUT: A STREAM OF DETECTED SYMBOLS
DE-SPREADER TYPE III
CHANNEL DECODER/ DEMODULATOR
ESTIMATED DATA SYMBOLS
2404
CHANNEL DECODER/DEMODULATOR
IN: A STREAM OF DETECTED SYMBOLS
OUT: A STREAM OF ESTIMATED DATA SYMBOLS

FIG. 24

MULTICODE SPREAD SPECTRUM COMMUNICATIONS SYSTEM

FIELD OF THE INVENTION

The invention deals with the field of multiple access communications using Spread Spectrum modulation. Multiple access can be classified as either random access, polling, TDMA, FDMA, CDMA or any combination thereof. Spread Spectrum can be classified as Direct Sequence, Frequency-Hopping or a combination of the two.

BACKGROUND OF THE INVENTION

Commonly used spread spectrum techniques are Direct Sequence Spread Spectrum (DSSS) and Code Division Multiple Access (CDMA) as explained respectively in Chapters 13 and 15 of "Digital Communication" by J. G. Proakis, Third Edition, 1995, McGraw Hill. DSSS (See Simon M. K. et al., "Spread Spectrum Communications Handbook," Revised Edition, McGraw-Hill, 1994 and see Dixon, R. C., "Spread Spectrum systems with commercial applications," Wiley InterScience, 1994) is a communication scheme in which information symbols are spread over code bits (generally called chips). It is customary to use noise-like codes called pseudo-random noise (PN) sequences. These PN sequences have the property that their auto-correlation is almost a delta function. In other words, proper codes perform an invertible randomized spreading of the information sequence. The advantages of this information spreading are:

1. The transmitted signal can be buried in noise and thus has a low probability of intercept.
2. The receiver can recover the signal from interferers (such as other transmitted codes) with a jamming margin that is proportional to the spreading code length.
3. DSSS codes of duration longer than the delay spread of the propagation channel can lead to multipath diversity implementable using a Rake receiver.
4. The FCC and Industry Canada have allowed the use of unlicensed low power DSSS systems of code lengths greater than or equal to 10 (part **15** rules) in some frequency bands (the ISM bands). It is the last advantage (i.e. advantage 4. above) that has given much interest recently to DSSS.

An obvious limitation of DSSS systems is the limited throughput they can offer. In any given bandwidth, W, a code of length M will reduce the effective bandwidth to W/M. To increase the overall bandwidth efficiency, system designers introduced Code Division Multiple Access (CDMA) where multiple DSSS communication links can be established simultaneously over the same frequency band provided each link uses a unique code that is noise-like, i.e. provided the cross-correlation between codes is almost null. Examples of CDMA is the next generation of digital Cellular communications in North America: "the TIA Interim Standard IS-95," (see QUALCOMM Inc., "An overview of the application of Code Division Multiple Access (CDMA) to digital cellular systems and personal cellular networks," May 21, 1992 and see Viterbi, A. J., "CDMA, Principles of Spread Spectrum Communications," Addison-Wesley, 1995) where a Base Station (BS) communicates to a number of Mobile Stations (MS) simultaneously over the same channel. The MSs share one carrier frequency during the mobile-to-base link (also known as the reverse link) which is 45 MHz away from the one used by the BS during the base-to-mobile link (also known as the forward link). During the forward link, the BS

transceiver is assigned N codes where N is less than or equal to M and M is the number of chips per DSSS code. During the reverse link each MS is assigned a unique code.

CDMA problems are:

1. The near-far problem on the reverse link: an MS transmitter "near" the BS receiver can overwhelm the reception of codes transmitted from other MSs that are "far" from the BS.
2. Synchronization on the reverse link: synchronization is complex (especially) if the BS receiver does not know in advance either the identity of the code being transmitted, or its time of arrival.

SUMMARY OF THE INVENTION

We have recognized that low power DSSS systems would be ideal communicators provided the problems of CDMA could be resolved. In order to avoid both the near-far problem and the synchronization problem that exist on the reverse link of a CDMA system, we have opted in this patent to use only the forward link at all times for MCSS Types I and II. This is achieved within a specified channel by allowing only one transceiver to transmit at a time within a certain coverage area. Such a transceiver is forced during transmission to act as the BS in transmit mode while the remaining transceivers are forced to act as MSs in receive mode. In this patent, we refer to such a modulation scheme as MultiCode Spread Spectrum (MCSS).

On the other hand, both the near-far problem and the synchronization problem that exist on the reverse link of a CDMA system are reduced drastically by using MCSS Type III. In this case, each user is assigned one code and each code is assigned a guard time such that it starts to transmit only after a given amount of time relative to any adjacent codes. By forcing the users to have separate start times, MCSS Type III forces the codes to be (quasi) orthogonal as long as the guard time between adjacent codes is long enough.

When viewed as DSSS, a MCSS receiver requires up to N correlators (or equivalently up to N Matched Filters) (such as in QUALCOMM Inc."An overview of the application of Code Division Multiple Access (CDMA) to digital cellular systems and personal cellular networks, May 21, 1994 and as in Viterbi, A. J., "CDMA, Principles of Spread Spectrum Communications," Addison-Wesley, 1995) with a complexity of the order of NM operations. When both N and M are large, this complexity is prohibitive. In addition, a nonideal communication channel can cause InterCode Interference (ICI), i.e. interference between the N SS codes at the receiver. In this patent, we introduce three new types of MCSS. MCSS Type I allows the information in a MCSS signal to be detected using a sequence of partial correlations with a combined complexity of the order of M operations. MCSS Type II allows the information in a MCSS signal to be detected in a sequence of low complexity parallel operations while reducing the ICI. MCSS Type III allows the information in a MCSS signal to be detected in a sequence of low complexity Multiply and Accumulate (MAC) operations implementable as a filter, which reduce the effect of multipath. In addition to low complexity detection and ICI reduction, our implementation of MCSS has the advantage that it is spectrally efficient since N can be made approximately equal to M. In DSSS, N=1 while in CDMA typically N<0.4M.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be better understood in conjunction with the appended drawings in which:

FIG. **1** illustrates a transmitter for MCSS Type I in which the signal in is VB data symbols in VBT seconds and the signal out is PM multicoded SS symbols in PMT_C seconds;

FIG. **2** provides a Spreader Type I (**104**) from FIG. **1**, in which the signal in is P frames of J modulated symbols each and the signal out is P frames of N spread spectrum symbols each, of length M chips per spread spectrum symbol;

FIG. **3** provides the ith computing means (**202**) from FIG. **2**, in which the signal in is the ith subset of modulated symbols and the signal out is the ith spread spectrum symbols of length M chips;

FIG. **4** provides the ith source (**302**) from FIG. **3** of L_i spread spectrum codes, in which the signal in is L_i preset sequences of length M chips each, and the signal out is L_i spread spectrum codes of length M chips each;

FIG. **5** provides the ith source (**302**) from FIG. **3** of L_i spread spectrum codes, in which the signal in is L_i preset values of length M chips each, and the signal out is L_i spread spectrum codes of length M chips each;

FIG. **6** is the Transmitter for MCSS Type II, in which the signal in is VB data symbols in VBT seconds and the signal out is PM multicoded SS symbols in PMT_C seconds;

FIG. **7** is the Spreader Type II (**604**) from FIG. **6**, in which the signal in is P frames of J modulated symbols each and the signal out is P frames of M multicoded SS symbols;

FIG. **8** is the ith M-point Transform (**702**) from FIG. **7**, in which the signal in is M subsets of modulated symbols and the signal out is M multicoded SS symbols;

FIG. **9** is the ith M-point Transform (**702**) from FIG. **7** in which the signal in is M subsets of modulated symbols and the signal out is M multicoded SS symbols;

FIG. **10** is the MCSS Transmitter Type III, in which the signal in is a stream of data symbols and the signal out is a stream of ramped multicoded SS symbols;

FIG. **11** is the Spreader (**1002**) Type III in FIG. **10**, in which the signal in is a sequence of modulated symbols and the signal out is a sequence of multicoded SS symbols;

FIG. **12** is the Randomizer (**1101**) in FIG. **11**, in which the signal in is a sequence of modulated symbols and the signal out is a sequence of randomized modulated symbols;

FIG. **13** is the Computing Means (**1102**) in FIG. **11**, in which the signal in is a sequence of randomized modulated symbols and the signal out is a sequence of multicoded SS symbols;

FIG. **14** is the Ramper (**1003**) in FIG. **10** for ramping the multicoded SS symbols using a linearly ramping carrier frequency, in which the signal in is a sequence of multicoded SS symbols and the signal out is a sequence of ramped multicoded SS symbols;

FIG. **15** is the Receiver for MCSS Type I & II, in which the signal in is PM multicoded SS symbols in PMT_C seconds and the signal out is VB estimated data symbols in VBT seconds;

FIG. **16** is the Despreader Type I (**1503**) from FIG. **15**, in which the signal in is P frames of M multicoded SS symbols each and the signal out is P frames of J despread symbols each;

FIG. **17** is the ith computing means (**1602**) from FIG. **16**, in which the signal in is M multicoded SS symbols and the signal out is ith computed value;

FIG. **18** is the Despreader Type II (**1503**) from FIG. **15**, in which the signal in is P frames of M multicoded SS symbols each and the signal out is P frames of J despread symbols each;

FIG. **19** is the Receiver for MCSS Type III, in which the signal in is a stream of multicoded SS symbols and the signal out is a stream of estimated data symbols;

FIG. **20** is the De-ramper (**1901**) in FIG. **19** for de-ramping the ramped multicoded SS symbols using a linearly de-ramping carrier frequency, in which he signal in is a steam of ramped multicoded SS symbols and the signal out is an estimated stream of multicoded SS symbols;

FIG. **21** is the De-Spreader (**1902**) Type III in FIG. **19**, in which the signal in is a sequence of multicoded SS symbols and the signal out is a sequence of detected symbols;

FIG. **22** is the Computing Means (**2101**) in FIG. **21**, in which the signal in is a stream of multicoded SS symbols and the signal out is a stream of randomized despread symbols;

FIG. **23** is the De-Randomizer (**2102**) in FIG. **21**, in which the signal in is a sequence of randomized despread data symbols and the signal out is a sequence of despread symbols; and

FIG. **24** is a preferred diversity receiver for MCSS Type III with de-ramping, in which the signal in is a stream of ramped multicoded SS symbols and the signal out is a stream of estimated data symbols.

DESCRIPTION OF THE INVENTION

The description of the invention consists of six parts. The first three parts correspond to the transmitter for each one of the three types of MCSS introduced in this patent, while the last three parts correspond to the receiver for each one of the three types of MCSS.

Description of the Transmitter for MCSS Type I:

FIG. **1** illustrates a block diagram of the transmitter for MCSS Type I with an input of V frames of B data symbols each, every VBT seconds and an output of P frames of M multicoded SS symbols each, every PMT_c seconds where T is the duration of one data symbol and T_c is the duration of one chip in a spread spectrum code. The data symbols can be either analog or digital. If digital, they belong to an alphabet of finite size. If analog, they correspond to the samples of an analog signal.

FIG. **1** is described as follows:

- The first block in FIG. **1** is a serial-to-parallel converter (**101**) with an input of B data symbols and an output of one frame of B data symbols, every BT seconds.
- The second block is a 2 Dimensional (2D) shift register (**102**) with an input of V frames of B data symbols each (input by shifting the frames from left to right V times) and an output of Q frames of B data symbols each, every VBT seconds.
- When the data symbols are analog, the third block (**103**) in FIG. **1** corresponds to an analog pulse modulator with several possible modulation schemes such as Pulse Amplitude Modulation (PAM), Pulse Position Modulation (PPM), Pulse Frequency Modulation (PFM), etc. When the data symbols are digital, the third block is a channel encoder/modulator (**103**) with an input of Q frames of B data symbols each and an output of P frames of J modulated symbols each, every QBT seconds. The channel encoder/modulator performs two functions: (1) to encode and (2) to modulate the data symbols. The first function offers protection to the symbols against a non ideal communication channel by adding redundancy to the input sequence of data symbols while the second function maps the protected symbols into constellation points that are appropriate to the communication channel. Sometimes it is possible to perform the two functions simultaneously such as in the case of Trellis Coded Modulation (TCM). For simplicity, we assume throughout the patent that the

two functions are performed simultaneously and refer to the block performing the two functions as the channel encoder/modulator.

Different types of channel encoders are available:

If the 2D shift register (**102**) is operated with V=Q, then the encoder performs block encoding, otherwise if V<Q, the encoder performs convolutional encoding. Furthermore, if B>J then the encoder is a trellis encoded modulator either with block encoding if V=Q or with convolutional encoding with V<Q.

If B=J, the code rate is Q/P, i.e. the encoder takes Q data symbols in and generates P encoded data symbols out where P>Q. Furthermore, if V<Q then (V−1) is the constraint length of the convolutional encoder.

If the 2D shift register (**102**) is operated with B>1, then it can act as an interleaver which interleaves the data symbols prior to the channel encoder (**103**), otherwise if B=1 the channel encoder does not rely on interleaving. Another possible form of interleaving is to interleave the coded data symbols after the channel encoder (not shown in FIG. **1**).

Different types of modulators are available such as: Binary Phase Shift Keying (BPSK), Quadrature Phase Shift Keying (QPSK), Multilevel Phase Shift Keying (MPSK), Quadrature Amplitude Modulation (QAM), Frequency Shift Keying (FSK), Continuous Phase Modulation (CPM), Amplitude Shift Keying (ASK), etc. All amplitude and frequency modulation schemes can be demodulated either coherently or noncoherently. All phase modulation schemes can de demodulated either coherently or differentially. In the latter case, differential encoding is required in the modulator such as in Differential BPSK (DBPSK), Differential QPSK (DQPSK), Differential MPSK (DMPSK), etc. Even though the output of the channel encoder/modulator (**103**) corresponds to an encoded and modulated data symbol, we will refer to it of as a 'modulated symbol'.

The fourth block is a spreader type I (**104**) with an input of P frames of J modulated symbols each and an output of P frames of N spread spectrum symbols each, of length M chips per spread spectrum symbol, every PMT_c seconds. The spreader type I (**104**) is explained further below in FIGS. **2–5**.

The fifth block is a 3 Dimensional (3D) shift register (**105**) with an input of P frames of N spread spectrum symbols each (input by shifting the PN symbols from inside to outside M chip times), and an output of M frames of N chips each (output by shifting MN chips from left to right P times) every PMT_c seconds.

The sixth block is a set of M adders (**106**). Each adder has an input of N chips and an output of one multicoded SS symbol, every MT_c seconds.

The seventh block is a parallel-to-serial converter (**107**) with an input of one frame of M multicoded SS symbol and an output of M multicoded SS symbol every MT_c seconds.

The spreader type I (**104**) in FIG. **1** is described further in FIG. **2** with an input of P frames of J modulated symbols each, generated by the channel encoder/modulator (**103**) in FIG. **1**, and an output of P frames of N spread spectrum symbols each, of length M chips per spread spectrum symbol. FIG. **2** is described as follows:

The first block in FIG. **2** is a set of P converters (**201**) with an input of one frame of J modulated symbols per converter, and an output of one frame of N subsets of modulated symbols per converter. The ith subset contains a number J_i of modulated symbols where $J_1+J_2+ \ldots +J_N=J$ and $i=1, \ldots, N$.

The second block is a set of N computing means (**202**) with an input of one subset of modulated symbols per computing means, and an output of one spread spectrum symbol, of length M chips per computing means.

The set of N computing means (**202**) in FIG. **2** is described further in FIG. **3** which displays only the ith computing mean where $i=1, \ldots, N$. The ith computing mean has as an input the ith subset of modulated symbols, and as an output the ith spread spectrum symbol of length M chips. FIG. **3** is described as follows.

The first block in FIG. **3** is the ith mapper (**301**) with two inputs and one output. The two inputs are: (1) the ith subset of modulated symbols which contains a number J_i of modulated symbols, and (2) L_i spread spectrum codes of length M chips each. The output is the ith spread spectrum symbol. The ith mapper chooses from the set of L_i spread spectrum codes the code corresponding to the ith subset of modulated symbols to become the ith spread spectrum code representing an invertible randomized spreading of the ith subset of modulated symbols.

The second block in FIG. **3** is the ith source (**302**) of L_i spread spectrum codes with an output of L_i spread spectrum codes of length M chips each. The ith source (**302**) can be thought of as either a lookup table or a code generator. Two different implementations of the ith source are shown in FIGS. **4** and **5**.

Remarks on the "invertible randomized spreading":

1. In this patent, the invertible randomized spreading of a signal using a spreader is only invertible to the extent of the available arithmetic precision of the machine used to implement the spreader. In other words, with finite precision arithmetic, the spreading is allowed to add a limited amount of quantization noise.
2. Moreover, the randomized spreading of a signal is not a perfect randomization of the signal (which is impossible) but only a pseudo-randomization. This is typical of spread spectrum techniques in general.
3. Finally, in some cases such as over the multipath communication channel, it is advantageous to spread the signal over a bandwidth wider than 25% of the coherence bandwidth of the channel. In this patent, we refer to such a spreading as wideband spreading. In the indoor wireless channel, 25% of the coherence bandwidth ranges from 2 MHz to 4 MHz. In the outdoor wireless channel, 25% of the coherence bandwidth ranges from 30 KHz to 60 KHz. In other words, in this patent wideband spreading corresponds to a spreading of the information signal over a bandwidth wider than 30 KHz over the outdoor wireless channel and wider than 2 MHz over the indoor wireless channel, regardless of the bandwidth of the information signal and regardless of the carrier frequency of modulation.

The ith source (**302**) of FIG. **3** can also be generated as in FIG. **4** as a set of L_i transforms with an input of one preset sequence of length M chips per transform and an output of one spread spectrum code of length M chips per transform. In other words, the ith source of spread spectrum codes could be either a look-up table containing the codes such as in FIG. **3** or a number of transforms generating the codes such as in FIG. **4**.

The ith source (**302**) of FIG. **3** can also be generated as in FIG. **5** as two separate blocks.

The first block (**501**) consists of a set of L_i transforms with an input of one preset sequence of length M chips per transform and an output of one spread spectrum code of length M chips per transform.

The second block is a randomizing transform (**502**) with an input of L_i transformed codes of length M chips each generated by the first block (**501**) and an output of L_i spread spectrum codes of length M chips each.

The randomizing transform consists of two parts. The first part is a randomizing look-up table (**503**) which contains a set of M preset values: $a_{1,i}, a_{2,i}, \ldots, a_{M,i}$. The second part multiplies each transformed symbol from the set of transformed symbols generated by the first transform (**501**) by the set of M preset values generated by the randomizing look-up table (**503**). The multiplication is performed chip-by-chip, i.e. the kth chip in the ith transformed symbol is multiplied by the kth value $a_{k,i}$ in the set of M preset values for all values of $k=1, \ldots, M$.

Description of the Transmitter for MCSS Type II:

FIG. **6** illustrates a block diagram of the transmitter for MCSS Type II with an input of VB data symbols every VBT seconds and an output of PM multicoded SS symbols every PMT_c seconds. FIG. **6** is described as follows:

The first block in FIG. **6** is a serial-to-parallel converter (**601**) with an input of B data symbols and an output of one frame of B data symbols, every BT seconds.

The second block is a 2 Dimensional (2D) shift register (**602**) with an input of V frames of B data symbols each (input by shifting the frames from left to right V times) and an output of Q frames of B data symbols each, every VBT seconds.

The third block is a channel encoder/modulator (**603**) with an input of Q frames of B data symbols each and an output of P frames of J modulated symbols each, every QBT seconds. The function of the channel encoder/modulator is exactly the same as the Channel encoder/modulator (**103**) described above for MCSS type I in FIG. **1**.

The fourth block is a spreader type II (**604**) with an input of P frames of J modulated symbols each and an output of P frames of M multicoded SS symbols each, every PMT_c seconds. The spreader type II is explained further below in FIGS. **7–9**.

The fifth block is a 2 Dimensional (2D) shift register (**605**) with an input of P frames of M multicoded SS symbols each, and an output of P frames of M multicoded SS symbols each (output by shifting the M frames from left to right P times) every PMT_c seconds.

The sixth block is a parallel-to-serial converter (**606**) with an input of one frame of M multicoded SS symbols and an output of M multicoded SS symbols every MT_c seconds.

The spreader type II (**604**) in FIG. **6** is described further in FIG. **7** with an input of P frames of J modulated symbols each, generated by the channel encoder/modulator (**603**) in FIG. **6**, and an output of P frames of M multicoded SS symbols each. FIG. **7** is described as follows:

The first block in FIG. **7** is a set of P converters (**701**) with an input of one frame of J modulated symbols per converter, and an output of one frame of M subsets of modulated symbols per converter. The ith subset contains a number of J_i of modulated symbols where $J_1+J_2+\ldots+J_M=J$ and $i=1, \ldots, M$.

The second block is a set of P M-point transforms (**702**) with an input of M subsets of modulated symbols per transform, and an output of a frame of M multicoded SS symbols per transform. The P M-point transforms perform the invertible randomized spreading of the M subsets of modulated symbols.

The set of P M-point transforms (**702**) in FIG. **7** is described further in FIG. **8** which displays only the ith M-point transform where $i=1, \ldots, N$. The input of the ith transform is the ith subset of J_i modulated symbols, and the output is the ith frame of M multicoded SS symbols. In FIG. **8**, the ith M-point transform is the randomizing transform (**801**) similar to the randomizing transform (**502**) in FIG. **5** with the set of preset values given as: $a_{1,i}, a_{2,i}, \ldots a_{M,i}$. In this case, the kth preset value $a_{k,i}$ multiplies the kth subset of J_k modulated symbols to generate the kth multicoded SS symbol.

The ith M-point transform (**801**) in FIG. **8** can further include a second M-point transform (**902**) as described in FIG. **9**.

The first M-point transform (**901**) is the ith randomizing transform with an input of the ith subset of J_i modulated symbols, and an output of the ith frame of M transformed symbols.

The second M-point transform (**902**) is the ith second M-point transform with an input of the ith frame of transformed symbols, and an output of the ith frame of M multicoded SS symbols.

Description of the Transmitter for MCSS Type II:

FIG. **10** illustrates a block diagram of the transmitter for MCSS Type III with an input of a stream of data symbols and an output of a stream of multicoded SS symbols. FIG. **10** is described as follows:

The first block is a channel encoder/modulator (**1001**) with an input of a stream of data symbols and an output of a stream of modulated symbols. The function of the channel encoder/modulator is similar to the channel encoder/modulator for MCSS types I and II (**103**) and (**603**) respectively except its operation is serial. Such a representation is commonly used in textbooks to implicitly imply that the data rate of the output stream of modulated symbols could be different from the input stream of data symbols. In other words, the channel encoder/modulator can add redundancy to the input stream of data symbols to protect it against channel distortion and noise. The type of redundancy varies depending on the type of encoding used. In block encoding, the redundancy depends only on the current block of data. In convolutional encoding, it depends on the current block and parts of the previous block of data. In both types of encoding trellis coding can be used which modulates the modulated symbols output from the encoder. Even though FIG. **10** does not contain an interleaver, it is possible to include one either before the channel encoder/modulator or after.

The second block is a spreader type III (**1002**) with an input of a stream of modulated symbols and an output of a stream of multicoded SS symbols. The spreader type III is further explained in FIGS. **11–13**.

The third block is a ramper (**1003**) with an input of multicoded SS symbols and an output of a ramped multicoded SS symbols. The ramper is further explained in FIG. **14**.

The spreader type III (**1002**) in FIG. **10** is described further in FIG. **11** as two blocks with an input of a stream of modulated symbols, generated by the channel encoder/modulator (**1001**) in FIG. **10**, and an output of a stream of multicoded SS symbols.

The first block is a randomizer (**1101**) with an input of a stream of modulated symbols and an output of a randomized modulated symbols. The randomizer is described further in FIG. **12**.

The second block is a computing means (**1102**) with an input of the stream of randomized modulated symbols and an output of a stream of multicoded SS symbols. The computing means is described further in FIG. **13**.

In FIG. **12** the randomizer (**1101**) from FIG. **11** is described further as two parts.

The first part is a chip-by-chip multiplier (**1201**) with two inputs and one output. The first input is the stream of modulated symbols and the second input is a stream of preset values output from a randomizing lookup table (**1202**). The output is the product between the two inputs obtained chip-by-chip, i.e. the kth randomized modulated symbols is obtained by multiplying the kth modulated symbol with the kth preset value a_k.

The second part is the randomizing lookup table (**1202**) which is the source of a stream of preset values: . . . ,a_k,a_{k+1}, . . . As mentioned before, the randomizing sequence is only pseudo-randomizing the modulated symbols.

In FIG. **13** the computing means (**1102**) from FIG. **11** is described further as a filter which performs the invertible randomized spreading of the stream of modulated symbols.

FIG. **14** illustrates the ramper (**1003**) in FIG. **10** as a mixer with two inputs and one output. The first input is the stream of multicoded SS symbols, the second input is a linearly ramping carrier frequency $e^{j2\pi f_o t^2}$ which ramps the multicoded SS stream over the time 't' thereby generating a stream of ramped multicoded SS symbols where $j=\sqrt{-1}$ and f_o is a constant.

Description of the Receiver for MCSS Type I:

FIG. **15** illustrates a block diagram of the receiver for MCSS type I & II with an input of PM multicoded SS symbols, every PMT_c seconds and an output of VB estimated data symbols, every VBT seconds. FIG. **15** is described as follows:

The first block in FIG. **15** is a serial-to-parallel converter (**1501**) with an input of M multicoded SS symbols and an output of one frame of M multicoded SS symbols every MT_c seconds.

The second block is a 2 Dimensional (2D) shift register (**1502**) with an input of one frame of M multicoded SS symbols each (input by shifting the frame from left to right P times) and an output of P frames of M multicoded SS symbols each, every PMT_c seconds.

The third block is a despreader type I (**1503**) with an input of P frames of M multicoded SS symbols each and an output of P frames of J despread symbols each every PMT_c seconds. The despreader type I is further explained below.

The fourth block is a channel decoder/demodulator (**1504**) with an input of P frames of J despread symbols each and an output of V frames of B estimated data symbols each, every VBT seconds. The channel decoder/demodulator performs two functions: (1) to map the despread symbols into protected data symbols and (2) either to detect errors, or to correct errors, or both. Sometimes, the two functions can be performed simultaneously. In this case, the channel decoder/demodulator performs soft-decision decoding, otherwise, it performs hard-decision decoding. By performing the two function, the channel encoder/demodulator accepts the despread symbols and generates estimated data symbols

The fifth block is a 2 Dimensional (2D) shift register (**1505**) with an input of V frames of B estimated data symbols each, and an output of V frames of B estimated data symbols (output by shifting the V frames from left to right) every VBT seconds. If the 2D shift register (**102**) is operated with B>1, then it might act as an interleaver. In this case, the receiver requires a de-interleaver which is accomplished using the 2D shift register (**1505**).

The sixth block is a parallel-to-serial converter (**1506**) with an input of one frame of B estimated data symbols and an output of B estimated data symbols, every VBT seconds.

The despreader type I (**1504**) in FIG. **15** is described further in FIG. **16** with an input of P frames of M multicoded SS symbols each from the received sequence of multicoded SS symbols, and an output of P frames of J despread symbols each. FIG. **16** is described as follows:

The first block in FIG. **16** is a set of P parallel-to-serial converters (**1601**) with an input of one frame of M multicoded SS symbols per converter, and an output of M multicoded SS symbols per converter.

The second block is a set of N computing means (**1602**) each having the same input of M multicoded SS symbols and an output of one computed value per computing means.

The third block is a detector (**1603**) with an input of N computed values and an output of J despread symbols per detector. When the data symbols are digital, the detector can make either hard decisions or soft decisions. When the data symbols are analog, L_i is necessarily equal to 1 for i=1, . . . , N and the detector is not required.

The set of N computing means (**1602**) in FIG. **16** is described further in FIG. **17** which displays only the ith computing mean where i=1, . . . , N. The ith computing mean has as an input the M multicoded SS symbols, and as an output the ith computed value. FIG. **17** is described as follows.

The first block in FIG. **17** is a set of L_i partial correlators (**1701**). The nth partial correlator has two inputs where n=1,2, . . . , L_i. The first input consists of the M multicoded SS symbols and the second input consists of the nth spread spectrum code of length M chips out of the ith source of L_i spread spectrum codes. The output of the nth partial correlator is the nth partially correlated value obtained by correlating parts of the first input with the corresponding parts of the second input.

The second block is the ith source (**1702**) of L_i spread spectrum codes with an output of L_i spread spectrum codes of length M chips each.

The third block is the ith sub-detector (**1703**) with an input of L_i partially correlated values and an output of the ith computed value. The ith sub-detector has two tasks. First using the L_i partially correlated values it has to obtain the full correlation between the M multicoded SS symbols and each one of the L_i spread spectrum codes of length M chips obtained from the ith source (**1702**). Then, it has to select the spread spectrum code corresponding to the largest correlation. Such a detected spread spectrum code together with the corresponding full correlation value form the ith computed value.

The detector (**1703**) in FIG. **16** takes all the computed values from each one of the N computing means and outputs J despread symbols. Based on the function of each sub-detector, one can say that the detector (**1603**) has two tasks at hand. First, it has to map each

detected spread spectrum code into a first set of despread symbols, then it has to map each full correlation value into a second set of despread symbols. In other words, the first set of despread symbols correspond to spread spectrum codes that form a subset of the spread spectrum codes corresponding to the second set of despread symbols.

It is also possible to have several layers of sub-detectors completing different levels of partial correlations and ending with N spread spectrum codes corresponding to the largest full correlation values per computing means. In this case, the tasks of the detector are first to map each detected spread spectrum code (obtained through the several layers of sub-detection) into sets of despread symbols, then to map each full correlation value into a final set of despread symbols.

Description of the Receiver for MCSS Type II:

FIG. **15** illustrates a block diagram of the receiver for MCSS Type II with an input of PM multicoded SS symbols every PMT_c seconds and an output of VB estimated data symbols every VBT seconds. FIG. **15** illustrates also the block diagram of the receiver for MCSS Type I and has been described above.

The despreader type II (**1504**) in FIG. **15** is described further in FIG. **18** with an input of P frames of M multicoded SS symbols each, and an output of P frames of J despread symbols each. FIG. **18** is described as follows:

The first block in FIG. **18** is a set of P M-point transforms (**1801**) with an input of one frame of M multicoded SS symbols per transformer, and an output of M transformed symbols per transformer.

The second block is a set of P detectors (**1802**) with an input of M transformed symbols per detector, and an output of J despread symbols per detector. Once again the detector can either make soft decisions or hard decisions.

Description of the Receiver for MCSS Type III:

FIG. **19** illustrates a block diagram of the receiver for MCSS Type III with an input of a stream of ramped multicoded SS symbols and an output of a stream of estimated data symbols. FIG. **19** is described as follows:

The first block in FIG. **19** is a de-ramper (**1901**) with an input of the stream of ramped multicoded SS symbols and an output of an estimated stream of multicoded SS symbols. The de-ramper is further described in FIG. **20**.

The second block is a de-spreader Type III (**1902**) with an input of the estimated stream of multicoded SS symbols and an output of a stream of detected symbols. The de-spreader type II is further explained in FIG. **21–23**.

The third block is a channel decoder/demodulator (**1903**) with the input consisting of the stream of detected symbols, and an output of a stream of estimated data symbols. It is clear from FIG. **19** that no de-interleaver is included in the receiver. As mentioned above, if an interleaver is added to the transmitter in FIG. **10**, then FIG. **19** requires a de-interleaver.

FIG. **20** illustrates the de-ramper (**1901**) in FIG. **19** as a mixer with two inputs and one output. The first input is the ramped multicoded SS symbols and the second input is a linearly ramping carrier frequency which deramps the ramped multicoded SS stream thereby generating an estimated stream of multicoded SS symbols.

The despreader type III (**1902**) in FIG. **19** is described further in FIG. **21** as three blocks.

The first block is a computing means (**2101**) with an input of an estimated stream of multicoded SS symbols and an output of a stream of randomized despread symbols. FIG. **22** describes the computing means (**2101**) in FIG. **21** as a filter (**2201**) which performs the despreading process.

The second block is a de-randomizer (**2102**) with an input of a stream of randomized despread symbols and an output of a stream of despread symbols. The de-randomizer (**2102**) is described further in FIG. **23**.

The third block is a detector (**2103**) with an input of a stream of despread symbols and an output of a stream of detected symbols. When the detector is a hard-decision detector it makes a decision on the despread symbols such that the detected values takes a finite number of values out of a predetermined alphabet of finite size. When the detector is a soft-decision detector the detected symbols are the same as the despread symbols.

The de-randomizer (**2102**) is described further in FIG. **23** as two parts.

The first part is a chip-by-chip multiplier (**2301**) with two inputs and an output. The first input is a stream of randomized despread data symbols and the second input is a stream of preset values output from a de-randomizing lookup table (**2302**). The output is the chip-by-chip product between the two inputs, i.e. the kth despread symbol is obtained as the product between the kth randomized despread symbol and the kth preset value b_k.

The second part is a de-randomizing lookup table (**2302**) which outputs a stream of preset values: . . . , b_k, b_{k+1}, . . .

Preferred Embodiments of the Invention:

From the above description of the invention, it is clear that the contribution of the invention is primarily in the spreader in the transmitter and in the despreader in the receiver for each one of the three type of MCSS introduced in the patent. The secondary contribution of the patent resides in the channel encoder/modulator and in the extra components that can be used in both the transmitter and in the receiver for each three types such as: the ramping and de-ramping of the signal and diversity techniques. For these reasons, we have separated the preferred embodiments of the invention into three parts. Each part corresponds to the spreader and the despreader for each one of the three types of MCSS and its extras.

Preferred Embodiments of the Spreader/Despreader for MCSS Type I:

In FIG. **1**, the spreader Type I (**104**) performs an invertible randomized spreading of the modulated symbols which carry either digital information or analog information, and in FIG. **15** the despreader Type I (**1503**) performs a reverse operation to the spreader Type I (**104**) within the limits of available precision (i.e. with some level of quantization noise).

In FIG. **1**, the spreader Type I (**104**) performs an invertible randomized spreading of the modulated, and in FIG. **15** the despreader Type I (**1503**) performs a reverse operation to the spreader Type I (**104**) while taking into account the effects of the communications channel such as noise, distortion and interference. The effects of the channel are sometimes unknown to the receiver (e.g. over selective fading channels which cause intersymbol interference). In such cases, the channel has to be estimated using for example a pilot signal known to the receiver as in "MultiCode Direct Sequence Spread Spectrum," by M. Fattouche and H. Zaghloul, U.S. Pat. No. 5,555,268, September 1996.

In FIG. **2**, if J_k=0 for any k=1, . . . , N then the output of the kth computing means is the all zeros spread spectrum codes of length M chips.

In FIG. **2**, if the modulated symbols are M-ary symbols, then a preferred value for L_i is M to the power of J_i. In other words, by choosing one spread spectrum code out of L_i codes, J_i symbols of information are conveyed.

In FIG. **3**, a preferred function for the ith mapper is to choose one spread spectrum code (out of the L_i available codes) based on one part of the ith subset of J_i modulated symbols while the second part of the subset is used to choose the symbol that multiplies the chosen spread spectrum code. In other words, assuming that the kth spread spectrum code S_k is chosen by the ith mapper **(301)** (out of the L_i available codes) based on the first part of the ith subset of J_i modulated symbols and that the symbol ξ is chosen to multiply S_k based on the second part of the ith subset of J_i modulated symbols, then the ith spread spectrum symbol out of the ith mapper **(301)** is $S_k\xi$. This is equivalent to spreading ξ over S_k.

In FIG. **3**, ξ can be chosen as a DBPSK symbol, a DQPSK symbol, a DMPSK symbol, a QAM symbol, a FSK symbol, a CPM symbol, an ASK symbol, etc.

In FIG. **3**, the L_i spread spectrum codes, out of the ith source **(302)** of L_i available spread spectrum codes, correspond to Walsh codes. Each Walsh code in FIG. **3** is generated in FIG. **4** as the output of an M-point Walsh transform where the input is a preset sequence of length M chips with (M-1) chips taking a zero value while one chip taking a unity value.

In FIG. **3**, the L_i spread spectrum codes, out of the ith source **(302)** of L_i available spread spectrum codes, correspond to randomized Walsh codes. Each Walsh code generated in FIG. **4** as the output of an M-point Walsh transform is randomized in FIG. **5** using a chip-by-chip multiplier where the kth chip of each Walsh code is multiplied by the preset value $a_{k,i}$ output from the ith randomizing lookup table.

In FIG. **5**, the M preset values $\{a_{1,i}, a_{2,i}, \ldots, a_{M,i}\}$ are chosen such that their amplitudes: $|a_{1,i}|, |a_{2,i}|, \ldots, |a_{M,i}|$ are all equal to unity.

In FIG. **3**, a preferred value for L_i is 2 and a preferred value for M is 10 with the two preferred spread spectrum codes out of the ith source **(302)** taking the values:

$$\{c_1, c_2, c_3, c_4, c_5, c_6, c_7, c_8, c_9, c_{10}\} \text{ and}$$
$$\{c_1, c_2, c_3, c_4, c_5, -c_6, -c_7, -c_8, -c_9, -c_{10}\} \tag{1}$$

In equation (1), preferred values for the chips '$c_1, c_2, c_3, c_4, c_5, c_6, c_7, c_8, c_9, c_{10}$' are '1,−,1,1,1,1,j,−j,j,j,j' which we refer to as the 'Wi-LAN codes Type I'.

Preferred Embodiments of the Spreader/Despreader for MCSS Type II:

In FIG. **6**, the spreader Type II **(604)** performs an invertible randomized spreading of the modulated symbols which carry either digital information or analog information, and in FIG. **15** the despreader Type II **(1503)** performs a reverse operation to the spreader Type II **(604)** within the limits of available precision (i.e. with some level of quantization noise).

In FIG. **6**, the spreader Type II **(604)** performs an invertible randomized spreading of the modulated, and in FIG. **15** the despreader Type II **(1503)** performs a reverse operation to the spreader Type II **(604)** while taking into account the effects of the communications channel such as noise, distortion and interference. As mentioned above, the effects of the channel are sometimes unknown to the receiver (e.g. over selective fading channels which cause intersymbol interference). In such cases, the channel has to be estimated using for example a pilot signal known to the receiver as in "MultiCode Direct Sequence Spread Spectrum," by M. Fattouche and H. Zaghloul, U.S. Pat. No. 5,555,268, September 1996.

Two preferred types of pilot signals can be used to estimate the effects of the channel on the information-bearing data symbols:

1. Pilot Frames inserted either before, during or after the Data frames of M multicoded SS symbols; and
2. Pilot Symbols inserted within each data frame of M multicoded SS symbols.

Pilot frames estimate the long term effects of the channel, while pilot symbols estimate the short term effects of the channel.

When channel estimation is used in the receiver as mentioned above, it is possible to use coherent detection with phase modulation, such as BPSK, QPSK and MPSK, after removing the effects of the channel from the phase of the received signal. On the other hand, if the effects of the channel are not removed, differential detection is selected instead with differentially-encoded phase modulation such as DPSK, DQPSK and DMPSK.

Furthermore, when channel estimation is used in the receiver as mentioned above, it is possible to use amplitude modulation together with coherent detection of phase modulation, such as ASK and QAM, after removing the effects of the channel from the phase and the amplitude of the received signal. On the other hand, if the effects of the channel are not removed, differential detection is selected instead with differentially-encoded phase and amplitude modulation such as Differential QAM using the star constellation.

A preferred modulation technique is QAM when the channel is estimated and its effects removed.

Another preferred modulation technique is DMPSK when the effects of the channel are not removed. In this case, a reference symbol is chosen at the beginning of each frame output from the channel modulator/modulator **(603)**.

In FIG. **6**, a preferred channel encoder/modulator **(603)** is a Reed-Solomon channel encoder used for encoding M-ary symbols and for correcting errors caused by the channel at the receiver. If the data symbols are binary, it is preferred to choose to combine several input bits into one symbol prior to encoding. A preferred technique to combine several bits into one symbol is to combine bits that share the same position within a number of consecutive frames. For example, the kth bit in the nth frame can be combined with the kth bit in the (n+1)th frame to form a dibit, where k=1, . . . , Q.

In FIG. **6**, if the data symbols are M-ary, a preferred value for B is unity when using a Reed-Solomon encoder, i.e. no interleaver is required in this case.

In FIG. **7**, preferred values for $J_1, J_2, \ldots, J_M$ are unity.

In FIG. **8**, preferred values for $\{a_{1,i}, a_{2,i}, \ldots, a_{M,i}\}$ are such that their amplitudes: $|a_{1,i}|, |a_{2,i}|, \ldots, |a_{M,i}|$ are all equal to unity.

In FIG. **9**, preferred ith second M-point transform (**902**) is a Discrete Fourier Transform (DFT).

When $J_1=J_2= \ldots =J_M=1$, $|a_{1,i}|=|a_{2,i}|= \ldots =|a_{M,i}|=1$ and the ith second M-point transform is a DFT, the MCSS transmitter is similar to the one in the issued patent: "Method and Apparatus for Multiple Access between Transceivers in Wireless Communications using OFDM Spread Spectrum," by M. Fattouche and H. Zaghloul, U.S. Pat. No. 5,282,222, Jan. 25 1994.

The generated spread spectrum codes using

$J_1=J_2= \ldots =J_M=1$,

$|a_{1,i}|=|a_{2,i}|= \ldots =|a_{M,i}|=1$,

the ith second M-point transform as a DFT, and

the channel encoder as a Reed-Solomon encoder without an interleaver are referred to as the 'Wi-LAN codes Type II'.

Another preferred embodiment of the ith second M-point transform (**902**) is a Circular FIR (CFIR) filter of length M coefficients which performs an M-point circular convolution between each block of M modulated symbols and its own coefficients. In this case, a preferred embodiment of the M-point transform (**1801**) is also a CFIR filter of length M coefficients which performs the inverse operation of the spreading CFIR filter by performing an M-point circular convolution between each block of M multicoded SS symbols and its own coefficients. When the channel is estimated, the despreading CFIR filter can also invert the effects of the channel using either

1. a linear algorithm such as Zero Forcing Equalization (ZFE) and Minimum Mean Square Equalization (MMSE); or
2. a nonlinear algorithm such as Decision Feedback Equalization (DFE) and Maximum Likelihood (ML).

The effect of a nonideal frequency-selective communication channel is to cause the multicodes to loose their orthogonality at the receiver. In the case when ZFE is employed, the CFIR filter acts as a decorrelating filter which decorrelates the M multicoded symbols from one another at the receiver thereby forcing the symbols to be orthogonal.

An advantage of using CFIR filter for spreading and despreading the data symbols is that IF-sampling can be inherently employed in the MCSS receiver without increasing the complexity of the digital portion of the receiver since interpolation and decimation filters can be included in the CFIR filters.

Preferred Embodiments of the Spreader/Despreader for MCSS Type III:

In FIG. **10**, the spreader Type III (**1002**) performs an invertible randomized spreading of the stream of modulated symbols which carry either digital information or analog information, and in FIG. **19** the despreader Type I (**1902**) performs a reverse operation to the spreader Type III (**1002**) within the limits of available precision (i.e. with some level of quantization noise).

In FIG. **10**, the spreader Type III (**1002**) performs an invertible randomized spreading of the stream of modulated symbols, and in FIG. **19** the despreader Type III (**1902**) performs a reverse operation to the spreader Type III (**1002**) while taking into account the effects of the communications channel such as noise, distortion and interference. As mentioned above, the effects of the channel are sometimes unknown to the receiver (e.g. over selective fading channels which cause intersymbol interference). In such cases, the channel has to be estimated using for example a pilot signal known to the receiver as in "MultiCode Direct Sequence Spread Spectrum," by M. Fattouche and H. Zaghloul, U.S. Pat. No. 5,555,268 September 1996.

A preferred randomizer (**1101**) in FIG. **11** is a trivial one with no effect on the modulated symbols.

Another preferred randomizer (**1101**) is one where the preset values out of the randomizing lookup table (**1202**): $\{\ldots, a_{k-1}, a_k, a_{k+1}, \ldots\}$ have amplitudes which are equal to unity.

In FIG. **13**, a preferred filter is a Finite Impulse Response (FIR) filter with the coefficients obtained as the values of a polyphase code.

In FIG. **13**, a preferred filter is an FIR filter with the coefficients obtained as approximations to the values of a polyphase code.

In FIG. **13**, a preferred filter is an FIR filter with the following 16 coefficients:

$$\{1,1,1,1,$$
$$1,j,-1,-j,$$
$$1,-1,1,-1,$$
$$1,-j,-1,j\}$$

forming its impulse response where $j=\sqrt{-1}$. The 16 coefficients correspond to the following polyphase code:

$$\{e^{j0\theta(0)}, e^{j1\theta(0)}, e^{j2\theta(0)}, e^{j3\theta(0)}, e^{j0\theta(1)}, e^{j1\theta(1)}, e^{j2\theta(1)}, e^{j3\theta(1)}, e^{j0\theta(2)}, e^{j\theta(2)}, e^{j2\theta(2)}, e^{j3\theta(2)}, e^{0\theta(3)}, e^{j\theta(3)}, e^{j2\theta(3)}, e^{j3\theta(3)}\}$$

where $\theta(0)=0$, $\theta(1)=2\pi/4$, $\theta(2)=4\pi/4$, $\theta(3)=6\pi/4$, and $j=\sqrt{-1}$.

In FIG. **13**, another preferred filter is an FIR filter with 64 coefficients corresponding to the following polyphase code:

$$\{e^{j0\theta(0)}, e^{j1\theta(0)}, e^{j2\theta(0)}, e^{j3\theta(0)}, e^{j4\theta(0)}, e^{j5\theta(0)}, e^{j6\theta(0)}, e^{j7\theta(0)}, e^{j0\theta(1)}, e^{j1\theta(1)}, e^{j2\theta(1)}, e^{j3\theta(1)}, e^{j4\theta(1)}, e^{j5\theta(1)}, e^{j6\theta(1)}, e^{j7\theta(1)}, e^{j0\theta(2)}, e^{j1\theta(2)}, e^{j2\theta(2)}, e^{j3\theta(2)}, e^{j4\theta(2)}, e^{j5\theta(2)}, e^{j6\theta(2)}, e^{j7\theta(2)}, e^{j0\theta(3)}, e^{j1\theta(3)}, e^{j2\theta(3)}, e^{j3\theta(3)}, e^{4\theta(3)}, e^{j5\theta(3)}, e^{j6\theta(3)}, e^{j7\theta(3)}, e^{j0\theta(4)}, e^{j1\theta(4)}, e^{j2\theta(4)}, e^{j3\theta(4)}, e^{j4\theta(4)}, e^{j5\theta(4)}, e^{j6\theta(4)}, e^{j7\theta(4)}, e^{j0\theta(5)}, e^{j1\theta(5)}, e^{j2\theta(5)}, e^{j3\theta(5)}, e^{j4\theta(5)}, e^{j5\theta(5)}, e^{j6\theta(5)}, e^{j7\theta(5)}, e^{j0\theta(6)}, e^{j1\theta(6)}, e^{j2\theta(6)}, e^{j3\theta(6)}, e^{j4\theta(6)}, e^{j5\theta(6)}, e^{j6\theta(6)}, e^{j7\theta(6)}, e^{j0\theta(7)}, e^{j1\theta(7)}, e^{j2\theta(7)}, e^{j3\theta(7)}, e^{j4\theta(7)}, e^{j5\theta(7)}, e^{j6\theta(7)}, e^{j7\theta(7)}\}$$

where $\theta(0)=0$, $\theta(1)=2\pi/8$, $\theta(2)=4\pi/8$, $\theta(3)=6\pi/8$, $\theta(4)=8\pi/8$, $\theta(5)=10\pi/8$, $\theta(6)=12\pi/8$, $\theta(7)=14\pi/8$, and $j=\sqrt{-1}$.

In general, a preferred filter in FIG. **13** with M coefficients corresponding to a polyphase code can be obtained as the concatenation of the rows of an $\sqrt{M}\times\sqrt{M}$ matrix (assuming $\sqrt{M}$ is an integer) with the coefficient in the ith row and kth column equal to $e^{j(i-1)\theta(k-1)}$ where $\theta(k)=2\pi k/\sqrt{M}$, and $j=\sqrt{-1}$.

Another preferred filter in FIG. **13** with M coefficients corresponding to a binary approximation of a polyphase code can be obtained as the concatenation of the rows of an $\sqrt{M}\times\sqrt{M}$ matrix with the coefficient in the ith row and kth column determined as follows:

when $(i-1)\theta(k-1)$ is an integer number of $\pi/2$, the coefficient is equal to $e^{j(i-1)\theta(k-1)}$ where $\theta(k)=2\pi k/\sqrt{M}$, otherwise

when $(i-1)\theta(k-1)$ is not an integer number of $\pi/2$, the coefficient is equal to $e^{jn\pi/2}$ where n is an integer number which minimizes the value: $(n\pi/2-(i-1)\theta(k-1))^2$.

We refer to the spread spectrum code corresponding to the coefficients of a filter representing a binary approximation of a polyphase code as discussed above as the 'Wi-LAN code Type III'. For example when M=64, the above procedure produces the following filter coefficients:

$$\{1, 1, 1, 1, 1, 1, 1, 1, 1, 1, j, j, -1, -1, -j, -j, 1, j, -1, -j, 1, j, -1, -j, 1, j, -j, 1, -1, -j, j, -1, 1, -1, 1, -1, 1, -1, 1, -1, 1, -1, j, -j, -1, 1, -j, j, 1, -j, -1, j, 1, -j, -1, j, 1, -j, -j, -1, -1, j, j, 1\}$$

A preferred filter in FIG. **21** performs a reverse operation to the filter (**1301**) in FIG. **13**.

Another preferred filter in FIG. **21** performs a matching filtering operation to the filter (**1301**) in FIG. **13**.

A preferred de-randomizer (**2102**) in FIG. **21** is one where the preset values out of the de-randomizing lookup table (**2302**): $\{\ldots, b_{k-1}, b_k, b_{k+1}, \ldots\}$ performs a reverse operation to the randomizer (**1101**) in FIG. **11**.

Another preferred de-randomizer (**2102**) in FIG. **21** is one where the preset values out of the de-randomizing lookup table (**2302**): $\{\ldots, b_{k-1,bk}, b_{k+1}, \ldots\}$ are equal to the reciprocal of the preset values out of the randomizing lookup table (**1202**) in FIG. **12**, i.e. $b_k=1/a_k$ for all values of k.

A preferred diversity technique for MCSS Type III is shown in FIG. **24** where we have L branches with one de-ramper (**2401**) per branch. Each de-ramper linearly de-ramps the received signal using a linearly deramping carrier frequency of fixed slope and unique intercept. Each intercept corresponds to a unique time of arrival of the different multipath components. The outputs of the L de-rampers are then combined in the combiner (**2402**) using any appropriate combining technique such as: co-phasing combining, maximum ratio combining, selection combining, equal gain combining, etc. The output of the combiner is then despread using the de-spreader (**2403**) and input into the channel decoder/demodulator (**2404**) to generate the estimated data symbols.

A preferred value for f_o in FIG. **14** is $1/(2\tau MT_c)$ where τ is the relative delay between the first arriving radio signal and the second arriving radio signal at the receiver, M is the number of coefficients in the spreading filter (**1301**) in FIG. **13** and T_c is the duration of one chip (or equivalently it is the unit delay in the spreading filter (**1301**)). In other words, the symbol rate at both the input and the output of the spreading filter (**1301**) is $1/T_c$.

The entire disclosure of U.S. Pat. Nos. 5,282,222 issued Jan. 25, 1994, and 5,555,268 issued Sep. 10, 1996, are hereby incorporated by reference in their entirety in this patent document.

A person skilled in the art could make immaterial modifications to the invention described in this patent document without departing from the essence of the invention that is intended to be covered by the scope of the claims that follow.

We claim:

1. A transceiver for transmitting a first stream of data symbols, the transceiver comprising:

a first converter for converting the first stream of data symbols into plural sets of B data symbols each;

a channel encoder/modulator for encoding plural sets of B data symbols into plural sets of J modulated symbols;

a spreader for spreading plural sets of J modulated symbols into plural sets of M multicoded SS symbols; and

a second converter for converting the plural sets of M multicoded SS symbols into a first stream of multicoded SS symbols for transmission, wherein the spreader includes:

a third converter for converting each one of the plural sets of J modulated symbols into M subsets of modulated symbols;

a transformer for operating on the M subsets of modulated symbols to generate M multicoded SS symbols as output, the M multicoded SS symbols corresponding to spreading each subset of modulated symbol over a separate spread spectrum symbol and combining the M spread spectrum symbols;

means for receiving a sequence of multicoded SS symbols, the multicoded SS symbols having been generated by spreading a second stream of data symbols, wherein the third converter converts the received stream of multicoded SS symbols into plural sets of M multicoded SS symbols each;

a despreader for despreading plural sets of M multicoded SS symbols to produce plural sets of J despread symbols in which the despreader includes:

a non trivial inverse transformer for inverse transforming M multicoded SS symbol from the received sequence of multicoded SS symbols into M transformed symbols; and

a detector for operating on the M transformed symbols to produce J despread symbols;

a channel decoder/demodulator for decoding plural sets of J despread symbols into plural sets of B estimated data symbols of the second stream of data symbols; and

a fourth converter for converting the plural sets of the B estimated data symbols into a stream of estimated data symbols of the second stream of data symbols.

2. The transceiver of claim **1** in which the non trivial inverse transformer:

inverse transforms M multicoded SS symbol from the received sequence of multicoded SS symbols into M transformed symbols; and

inverts the effects of the channel using either the pilot symbols or the pilot frames or both, relying either on a linear algorithm or on a nonlinear algorithm.

3. The transceiver of claim **1** in which the non trivial inverse transformer corresponds to a circular finite impulse response filter.

4. A transceiver for transmitting a first stream of data symbols, the transceiver comprising:

a channel encoder/modulator for encoding the first stream of data symbols into a modulated stream;

a spreader for spreading the modulated stream into a multicoded SS stream corresponding to an invertible randomized spreading of the modulated stream;

means to ramp the multicoded SS stream using a linearly ramping carrier frequency, thereby generating a stream of ramped multicoded SS symbols;

means for receiving a stream of ramped multicoded SS symbols, the ramped multicoded SS symbols having

been generated by encoding and invertible randomized spreading of a second stream of data symbols;

a de-ramper for de-ramping the ramped multicoded SS symbols from the received stream of ramped multicoded SS symbols using a linearly de-ramping carrier frequency thereby generating an estimate of the stream of multicoded SS symbols;

a despreader for despreading the estimated stream of multicoded SS symbols into a detected stream; and

a channel decoder/demodulator for decoding the detected stream to produce an estimate of the second stream of data symbols.

5. The transceiver of claim **4** in which the despreader comprises:

a filter for despreading the estimated sequence of multicoded SS symbols into an estimated stream of randomized despread data symbols;

a de-randomizer for de-randomizing the estimated stream of randomized despread data symbols into an estimated stream of despread multicoded SS symbols; and

a detector for detecting the estimated stream of despread symbols thereby generating a stream of detected symbols.

6. The transceiver of claim **5** further including;

means to apply diversity reception to the received sequence of ramped multicoded SS symbols; and

means to combine received diversity signals.

7. The transceiver of claim **6** in which the diversity reception is a multipath diversity reception where each diversity branch uses a different filter for despreading the estimated stream of multicoded SS symbols.

8. A method of exchanging data streams between a plurality of transceivers, the method comprising the steps of:

converting a first stream of data symbols into plural sets of B data symbols each;

channel encoding plural sets of B data symbols into plural sets of J modulated symbols;

spreading plural sets of J modulated symbols into plural sets of M multicoded SS symbols including:

converting each one of the plural sets of J modulated symbols into M subsets of modulated symbols; and

transforming, by way of a transform, the M subsets of modulated symbols to generate M multicoded SS symbols as output, the M multicoded SS symbols corresponding to spreading each subset of modulated symbol over a separate spread spectrum symbol and combining the M spread spectrum symbols;

converting the plural sets of M multicoded SS symbols into a first stream of multicoded SS symbols for transmission;

transmitting the multicoded SS symbols from a first transceiver at a time when no other of the plurality of transceivers is transmitting;

receiving, at a transceiver distinct from the first transceiver, the sequence of multicoded SS symbols;

converting the received stream of multicoded SS symbols into plural sets of M multicoded SS symbols each;

despreading plural sets of M multicoded SS symbols to produce plural sets of J despread symbols including the steps of:

inverse transforming, by application of an inverse transform, each multicoded SS symbol from the received sequence of multicoded SS symbols; and

operating on the M transformed symbols through the use of a detector to produce J despread symbols;

decoding plural sets of J despread symbols into plural sets of B estimated data symbols of the first stream of data symbols; and

converting the plural sets of the B estimated data symbols into a stream of estimated data symbols of the first stream of data symbols.

9. The method of claim **8** in which inverse transforming, by application of an inverse transform, each multicoded SS symbol from the received sequence of multicoded SS symbols includes a circular convolution.

10. A method of exchanging data streams between a plurality of transceivers, the method comprising the steps of:

channel encoding a first stream of data symbols into a stream of modulated symbols;

spreading the stream of modulated symbols to produce a multicoded SS stream corresponding to an invertible randomized spreading of the first modulated stream;

ramping the multicoded SS stream using a linearly ramping carrier frequency, thereby generating a stream of ramped multicoded SS symbols;

receiving, at a transceiver distinct from the first transceiver, the stream of ramped multicoded SS symbols;

de-ramping the ramped multicoded SS stream using a linearly deramping carrier frequency to produce an estimate of the multicoded SS stream;

despreading the estimated stream of multicoded SS symbols to produce a detected stream; and

decoding the detected stream to produce an estimate of the first stream of data symbols.

11. The method of claim **10** in which despreading the sequence of multicoded SS symbols to produce a despread stream comprises:

filtering the estimated stream of multicoded SS symbols, through the use of a filter, to generate an estimated stream of randomized despread symbols;

de-randomizing through the use of a de-randomizer the estimated stream of randomized despread symbols to generate an estimated stream of despread symbols; and

detecting the estimated stream of despread data symbols through the use of a detector to obtain a stream of detected symbols.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,192,068 B1

DATED : February 20, 2001

INVENTOR(S) : M.T. Fattouche et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page,

Item [56], **References Cited**, U.S. PATENT DOCUMENTS, insert in appropriate numerical order the following:

-- 5,228,025 7/1993 Le Flock et al. --

Signed and Sealed this

Twenty-ninth Day of April, 2003

JAMES E. ROGAN

Director of the United States Patent and Trademark Office

EXHIBIT C

US006320897B1

(12) **United States Patent**
Fattouche et al.

(10) **Patent No.: US 6,320,897 B1**
(45) **Date of Patent: *Nov. 20, 2001**

(54) **MULTICODE SPREAD SPECTRUM COMMUNICATIONS SYSTEM**

(75) Inventors: **Michel T. Fattouche**; **Hatim Zaghloul**; **Paul R. Milligan**; **David L. Snell**, all of Calgary (CA)

(73) Assignee: **Wi-LAN Inc.**, Calgary (CA)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/389,394**

(22) Filed: **Sep. 3, 1999**

Related U.S. Application Data

(63) Continuation of application No. 08/725,556, filed on Oct. 3, 1996, now Pat. No. 6,192,068.

(51) **Int. Cl.**[7] **H04B 15/00**
(52) **U.S. Cl.** **375/130**
(58) **Field of Search** 375/130, 140, 375/139, 146, 147, 150

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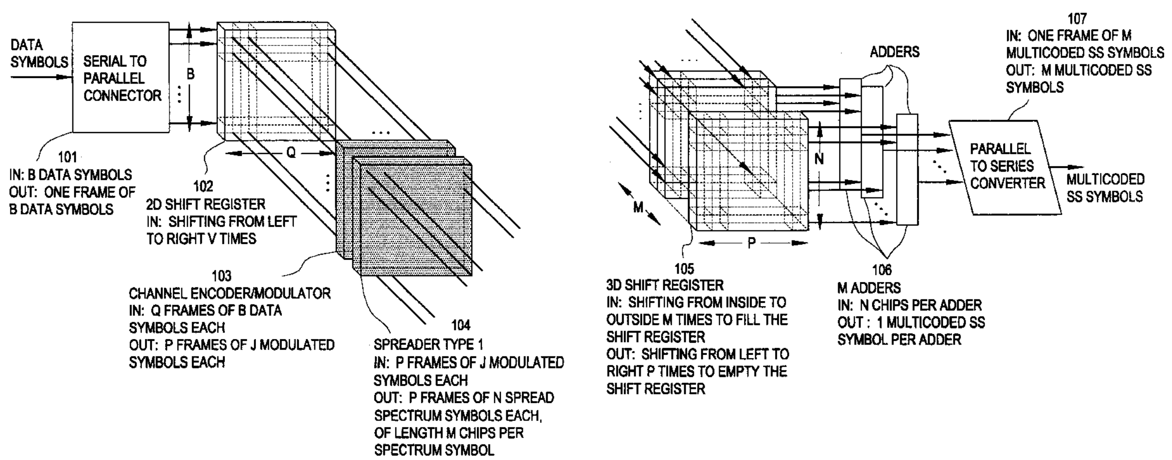
Primary Examiner—Chi Pham
Assistant Examiner—Khai Tran
(74) *Attorney, Agent, or Firm*—Christensen O'Connor Johnson Kindness PLLC

(57) **ABSTRACT**

MultiCode Spread Spectrum (MCSS) is a modulation scheme that assigns a number N of Spread Spectrum (SS) codes to an individual user where the number of chips per SS code is M. When viewed as Direct Sequence Spread Spectrum, MCSS requires up to N correlators (or equivalently up to N Matched Filters) at the receiver with a complexity of the order of NM operations. In addition, a non ideal communication channel can cause InterCode Interference (ICI), i.e. interference between the N SS codes. In this patent, we introduce three new types of MCSS. MCSS Type I allows the information in a MCSS signal to be detected using a sequence of partial corrrelations with a combined complexity of the order of M operations. MCSS Type II allows the information in a MCSS signal to be detected in a sequence of low complexity parallel operations which reduce the ICI. MCSS Type III allows the information in a MCSS signal to be detected using a filter suitable for ASIC implementation or on Digital Signal Processor, which reduces the effect of multipath. In addition to low complexity detection and reduced ICI, MCSS has the added advantage that it is spectrally efficient.

46 Claims, 22 Drawing Sheets



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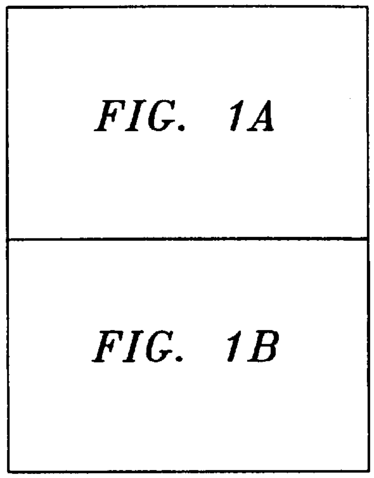


FIG. 1A
FIG. 1B

FIG. 1

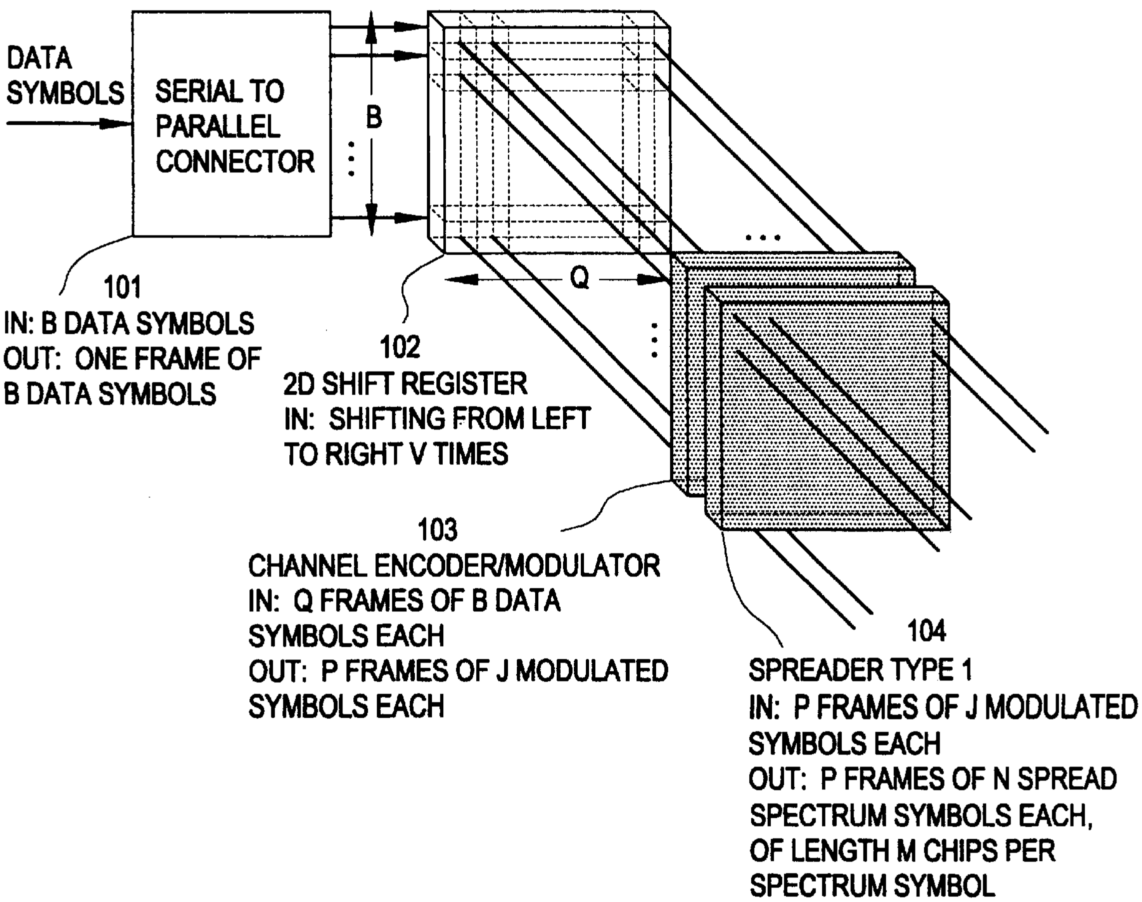
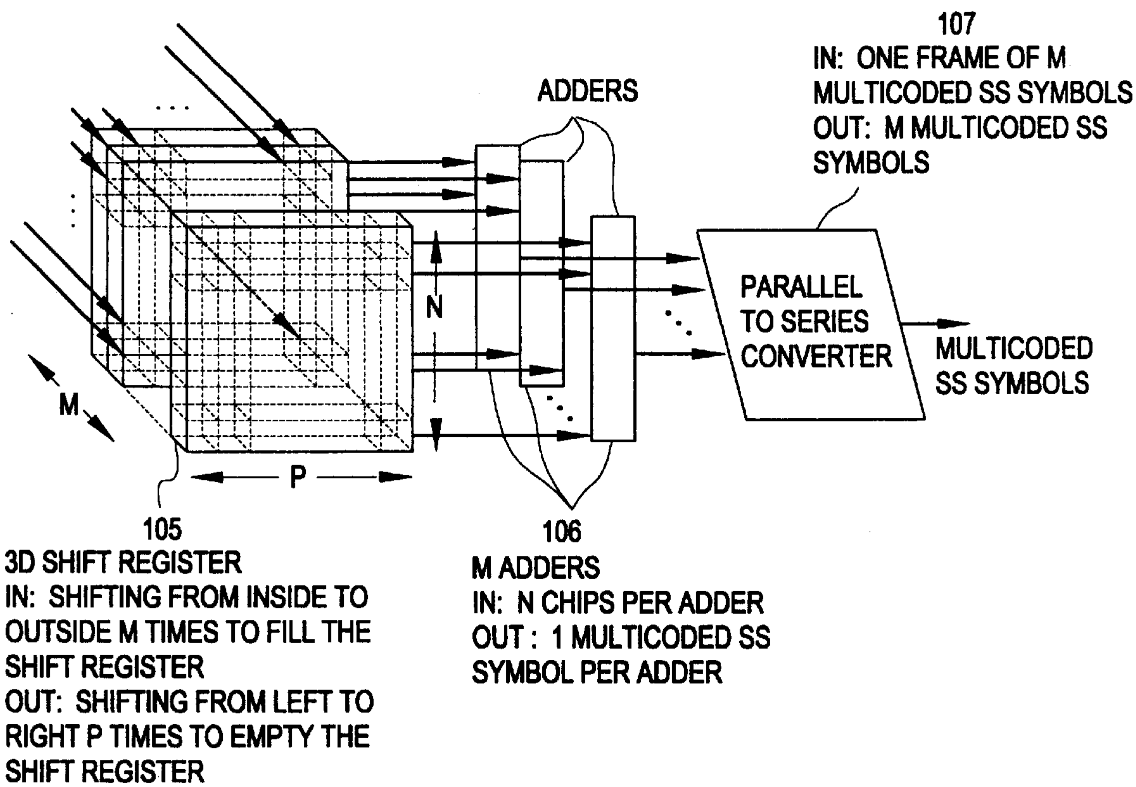
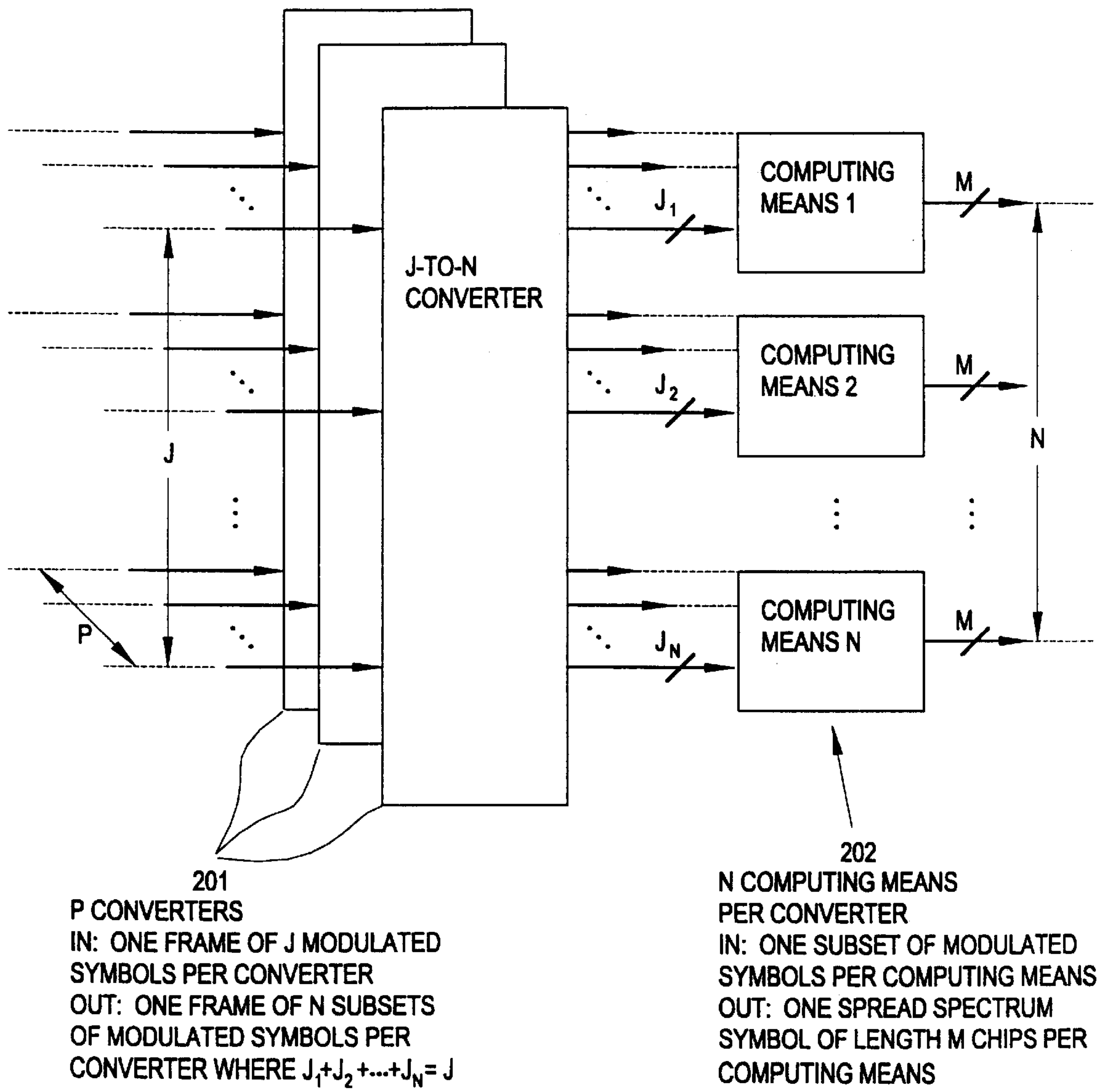

DATA
SYMBOLS
SERIAL TO
PARALLEL
CONNECTOR
B
Q
101
IN: B DATA SYMBOLS
OUT: ONE FRAME OF
B DATA SYMBOLS
102
2D SHIFT REGISTER
IN: SHIFTING FROM LEFT
TO RIGHT V TIMES
103
CHANNEL ENCODER/MODULATOR
IN: Q FRAMES OF B DATA
SYMBOLS EACH
OUT: P FRAMES OF J MODULATED
SYMBOLS EACH
104
SPREADER TYPE 1
IN: P FRAMES OF J MODULATED
SYMBOLS EACH
OUT: P FRAMES OF N SPREAD
SPECTRUM SYMBOLS EACH,
OF LENGTH M CHIPS PER
SPECTRUM SYMBOL

FIG. 1A

FIG. 1B

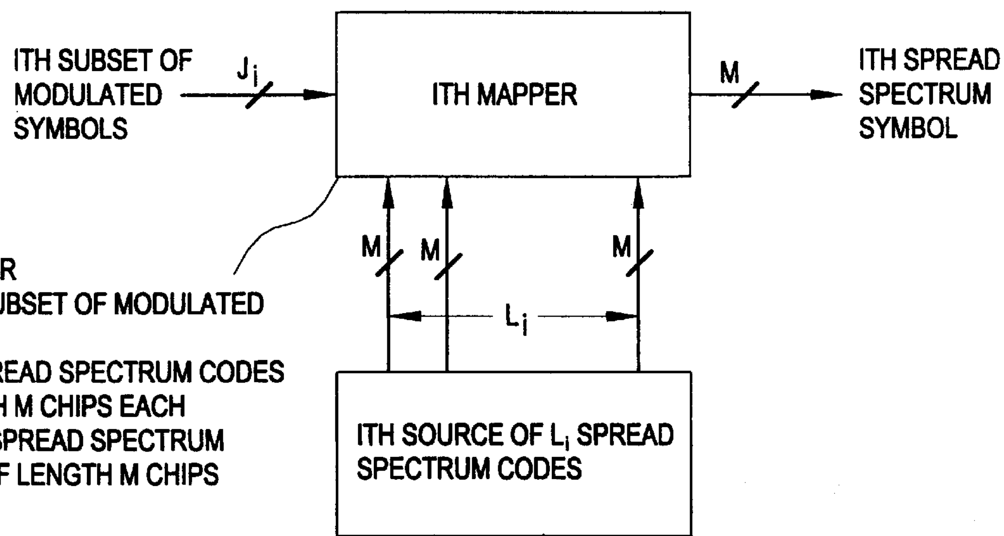

107
IN: ONE FRAME OF M MULTICODED SS SYMBOLS
OUT: M MULTICODED SS SYMBOLS
ADDERS
N
M
P
PARALLEL TO SERIES CONVERTER
MULTICODED SS SYMBOLS
105
3D SHIFT REGISTER
IN: SHIFTING FROM INSIDE TO OUTSIDE M TIMES TO FILL THE SHIFT REGISTER
OUT: SHIFTING FROM LEFT TO RIGHT P TIMES TO EMPTY THE SHIFT REGISTER
106
M ADDERS
IN: N CHIPS PER ADDER
OUT : 1 MULTICODED SS SYMBOL PER ADDER



J-TO-N
CONVERTER
COMPUTING MEANS 1
COMPUTING MEANS 2
COMPUTING MEANS N
J_1
J_2
J_N
M
M
M
N
J
P
201
P CONVERTERS
IN: ONE FRAME OF J MODULATED SYMBOLS PER CONVERTER
OUT: ONE FRAME OF N SUBSETS OF MODULATED SYMBOLS PER CONVERTER WHERE $J_1+J_2+...+J_N=J$
202
N COMPUTING MEANS PER CONVERTER
IN: ONE SUBSET OF MODULATED SYMBOLS PER COMPUTING MEANS
OUT: ONE SPREAD SPECTRUM SYMBOL OF LENGTH M CHIPS PER COMPUTING MEANS

FIG. 2

FIG. 3



301
ITH MAPPER
IN1: ITH SUBSET OF MODULATED SYMBOLS
IN2: L_i SPREAD SPECTRUM CODES OF LENGTH M CHIPS EACH
OUT: ITH SPREAD SPECTRUM SYMBOL OF LENGTH M CHIPS

302
ITH SOURCE OF L_i SPREAD SPECTRUM CODES
OUT: L_i SPREAD SPECTRUM CODES OF LENGTH M CHIPS EACH

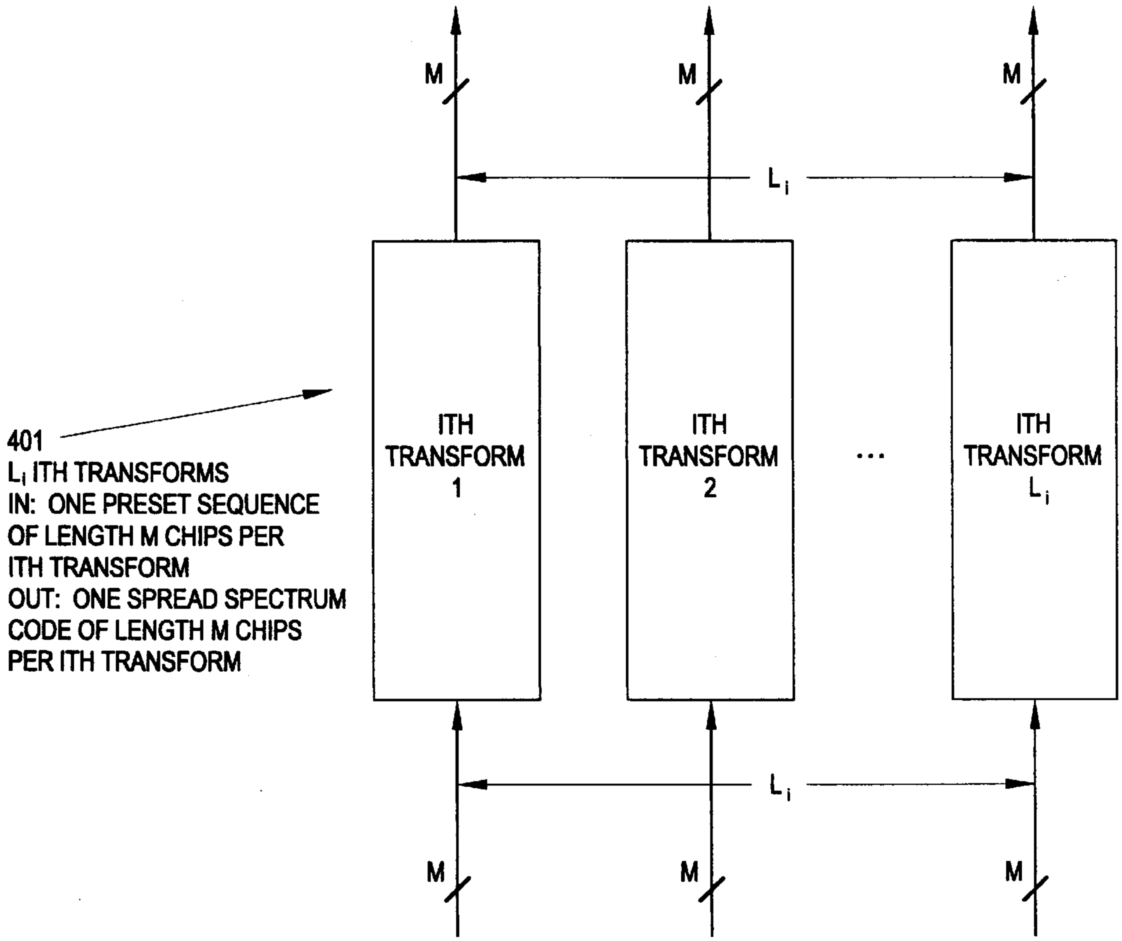
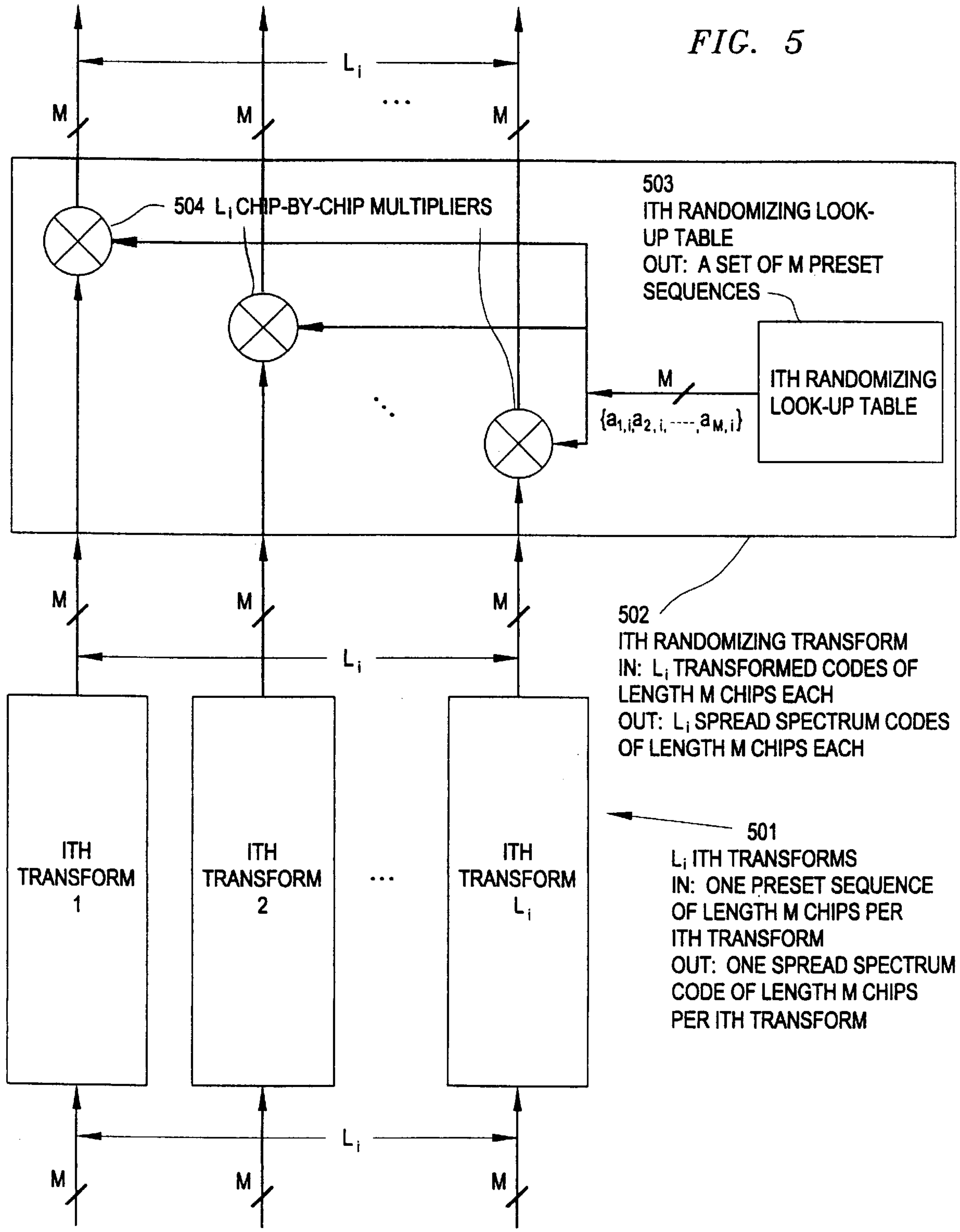

401
L_i ITH TRANSFORMS
IN: ONE PRESET SEQUENCE OF LENGTH M CHIPS PER ITH TRANSFORM
OUT: ONE SPREAD SPECTRUM CODE OF LENGTH M CHIPS PER ITH TRANSFORM
M
M
M
L_i
ITH TRANSFORM 1
ITH TRANSFORM 2
...
ITH TRANSFORM L_i
L_i
M
M
M

FIG. 4

FIG. 5



L_i
M
M
M
504 L_i CHIP-BY-CHIP MULTIPLIERS
503
ITH RANDOMIZING LOOK-UP TABLE
OUT: A SET OF M PRESET SEQUENCES
M
$\{a_{1,i}, a_{2,i}, ----, a_{M,i}\}$
ITH RANDOMIZING LOOK-UP TABLE
M
M
M
L_i
502
ITH RANDOMIZING TRANSFORM
IN: L_i TRANSFORMED CODES OF LENGTH M CHIPS EACH
OUT: L_i SPREAD SPECTRUM CODES OF LENGTH M CHIPS EACH
ITH TRANSFORM 1
ITH TRANSFORM 2
ITH TRANSFORM L_i
501
L_i ITH TRANSFORMS
IN: ONE PRESET SEQUENCE OF LENGTH M CHIPS PER ITH TRANSFORM
OUT: ONE SPREAD SPECTRUM CODE OF LENGTH M CHIPS PER ITH TRANSFORM
L_i
M
M
M

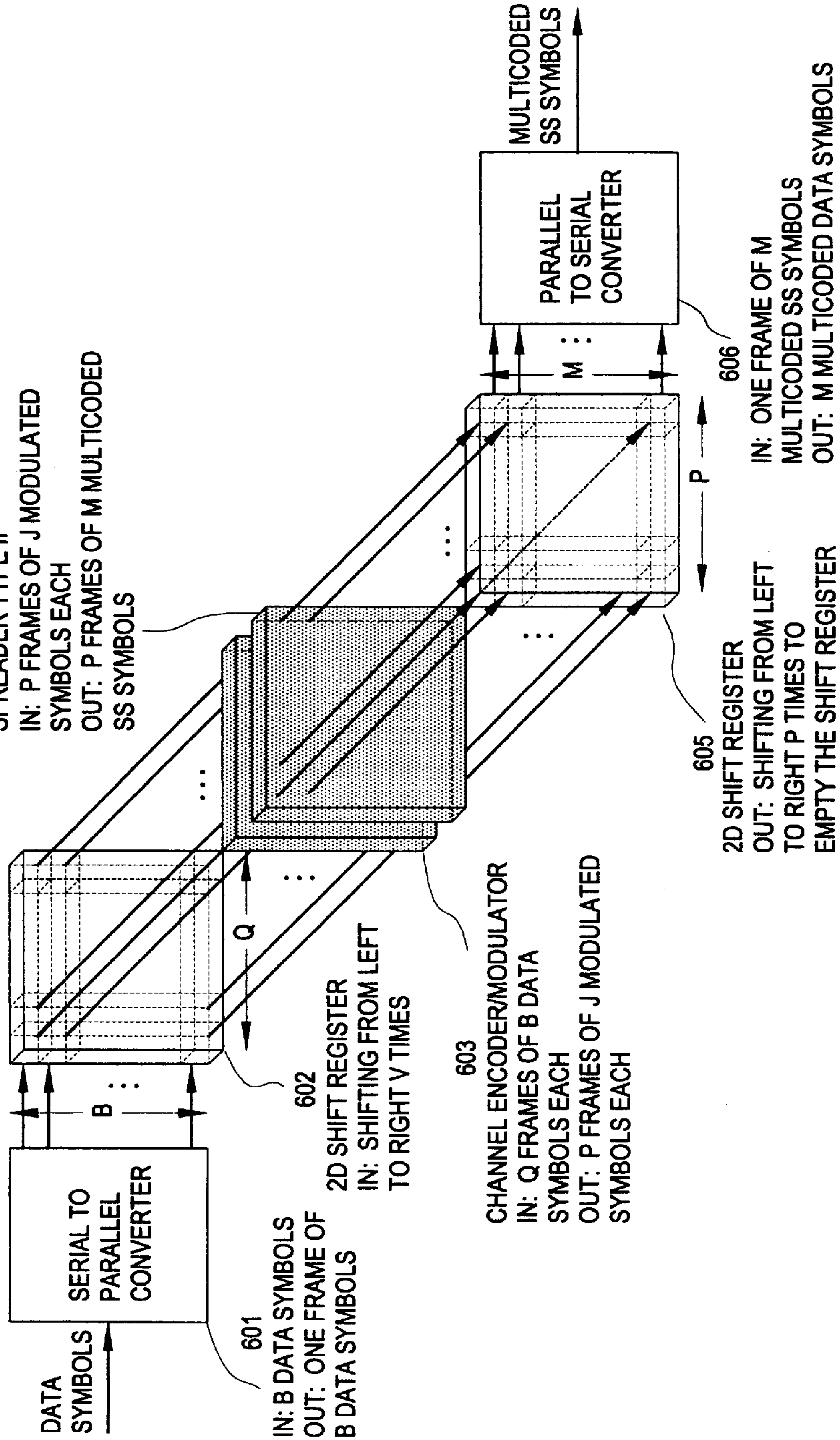

DATA SYMBOLS
SERIAL TO PARALLEL CONVERTER
601
IN: B DATA SYMBOLS
OUT: ONE FRAME OF B DATA SYMBOLS
B
602
2D SHIFT REGISTER
IN: SHIFTING FROM LEFT TO RIGHT V TIMES
Q
603
CHANNEL ENCODER/MODULATOR
IN: Q FRAMES OF B DATA SYMBOLS EACH
OUT: P FRAMES OF J MODULATED SYMBOLS EACH
604
SPREADER TYPE II
IN: P FRAMES OF J MODULATED SYMBOLS EACH
OUT: P FRAMES OF M MULTICODED SS SYMBOLS
605
2D SHIFT REGISTER
OUT: SHIFTING FROM LEFT TO RIGHT P TIMES TO EMPTY THE SHIFT REGISTER
P
M
PARALLEL TO SERIAL CONVERTER
606
IN: ONE FRAME OF M MULTICODED SS SYMBOLS
OUT: M MULTICODED DATA SYMBOLS
MULTICODED SS SYMBOLS

FIG. 6

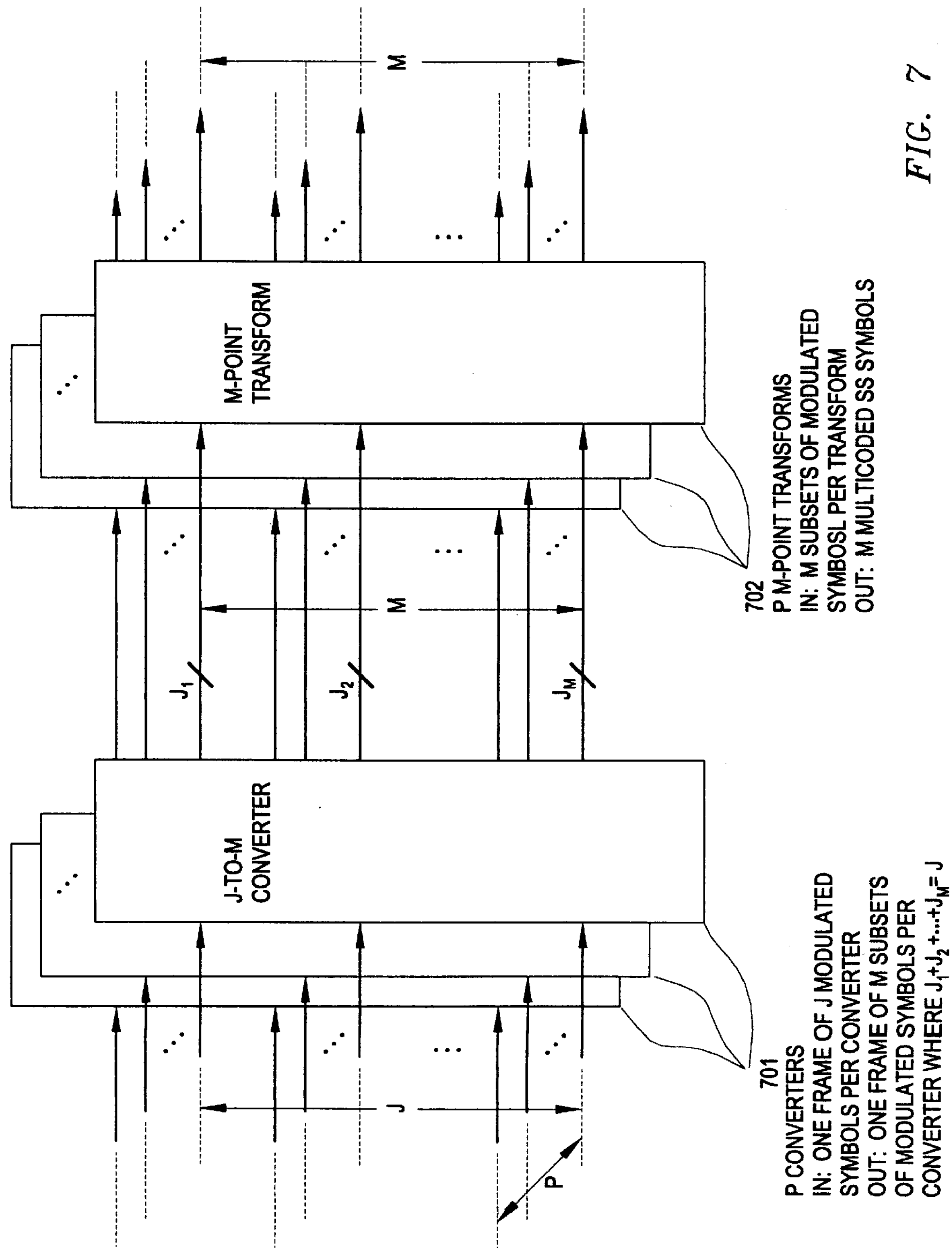
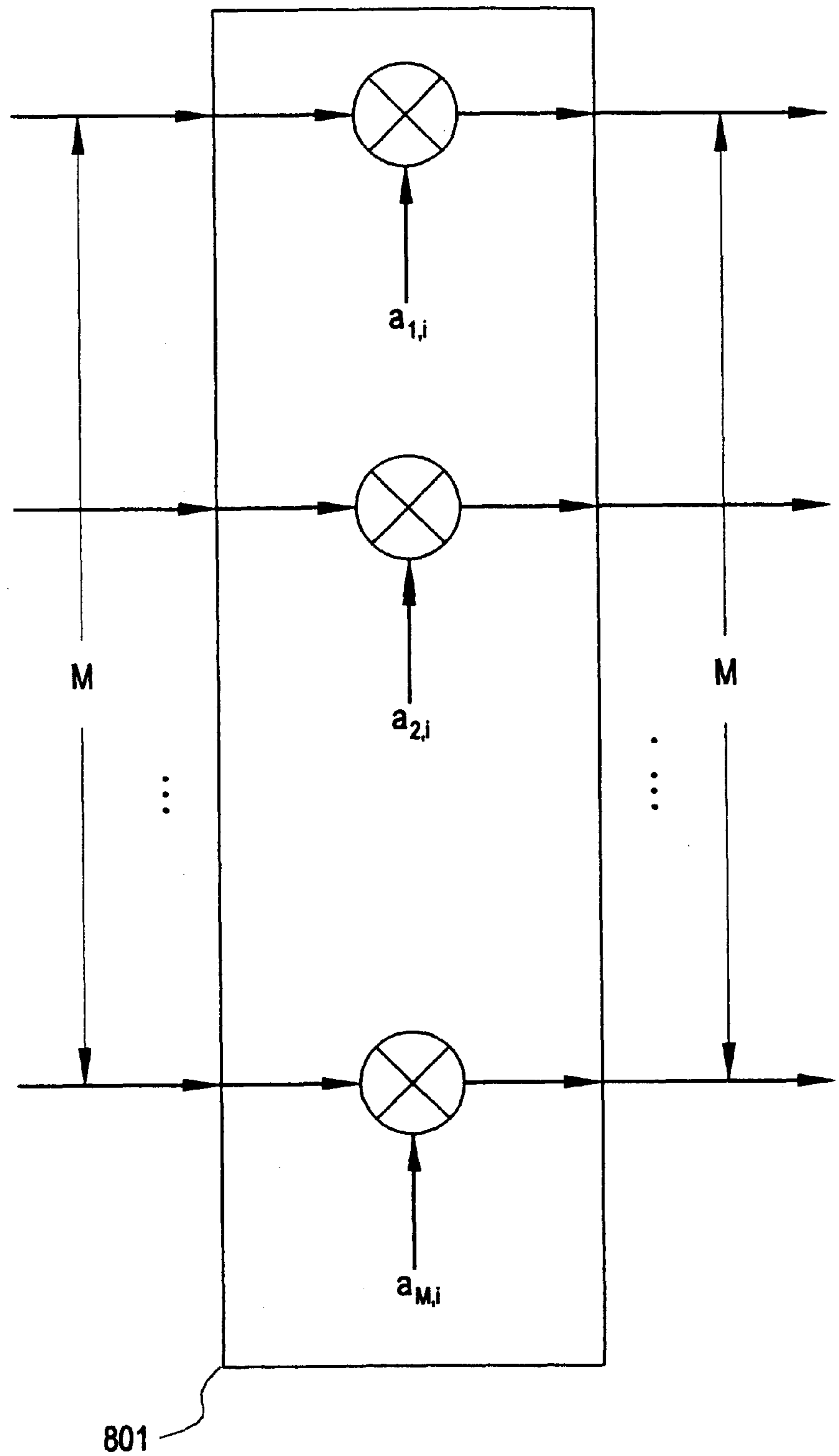

M
M-POINT TRANSFORM
M
J_1
J_2
J_M
J-TO-M CONVERTER
J
P
702
P M-POINT TRANSFORMS
IN: M SUBSETS OF MODULATED SYMBOSL PER TRANSFORM
OUT: M MULTICODED SS SYMBOLS
701
P CONVERTERS
IN: ONE FRAME OF J MODULATED SYMBOLS PER CONVERTER
OUT: ONE FRAME OF M SUBSETS OF MODULATED SYMBOLS PER CONVERTER WHERE $J_1+J_2+...+J_M=J$

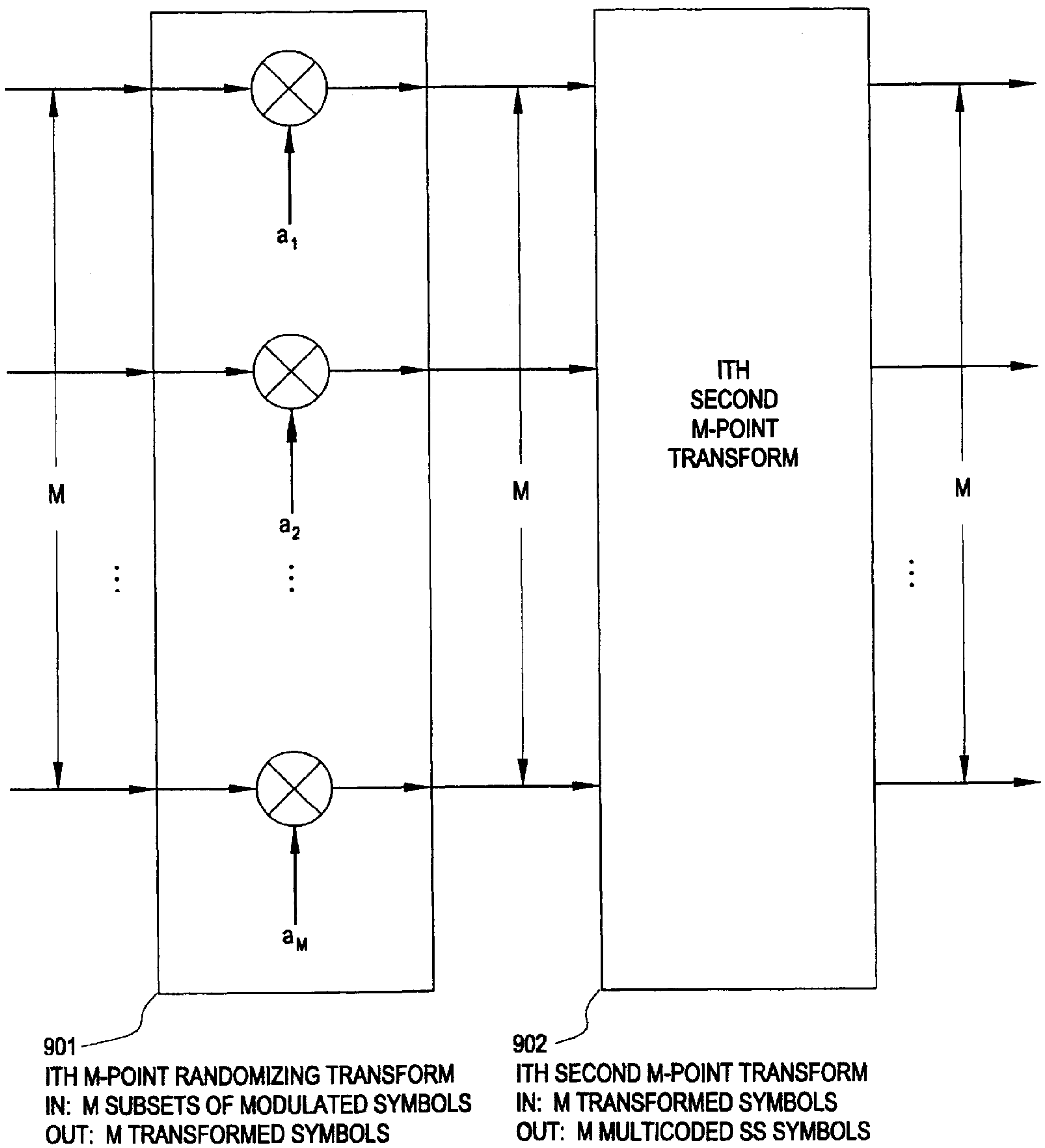
FIG. 7

FIG. 8



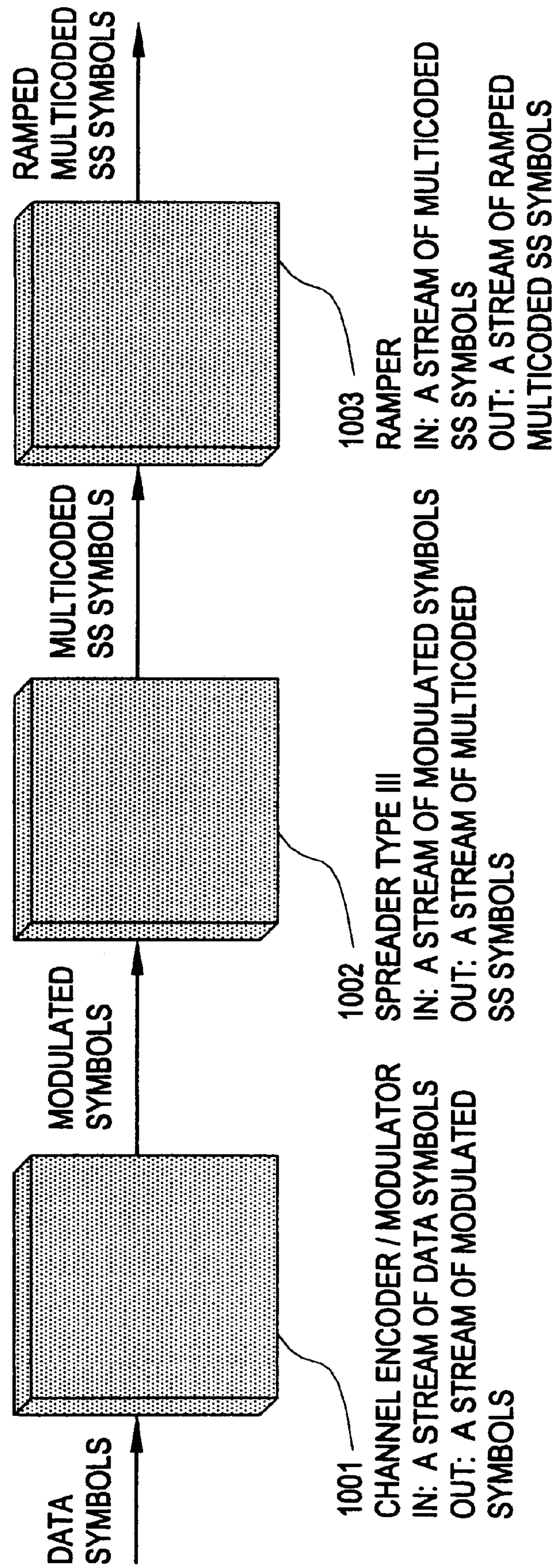
ITH M-POINT RANDOMIZING TRANSFORM
IN: M SUBSETS OF MODULATED SYMBOLS
OUT: M MULTICODED SS SYMBOLS

FIG. 9



a_1
a_2
a_M
M
M
M
ITH SECOND M-POINT TRANSFORM
901
ITH M-POINT RANDOMIZING TRANSFORM
IN: M SUBSETS OF MODULATED SYMBOLS
OUT: M TRANSFORMED SYMBOLS
902
ITH SECOND M-POINT TRANSFORM
IN: M TRANSFORMED SYMBOLS
OUT: M MULTICODED SS SYMBOLS

FIG. 10


DATA SYMBOLS
1001
CHANNEL ENCODER / MODULATOR
IN: A STREAM OF DATA SYMBOLS
OUT: A STREAM OF MODULATED SYMBOLS
MODULATED SYMBOLS
1002
SPREADER TYPE III
IN: A STREAM OF MODULATED SYMBOLS
OUT: A STREAM OF MULTICODED SS SYMBOLS
MULTICODED SS SYMBOLS
1003
RAMPER
IN: A STREAM OF MULTICODED SS SYMBOLS
OUT: A STREAM OF RAMPED MULTICODED SS SYMBOLS
RAMPED MULTICODED SS SYMBOLS

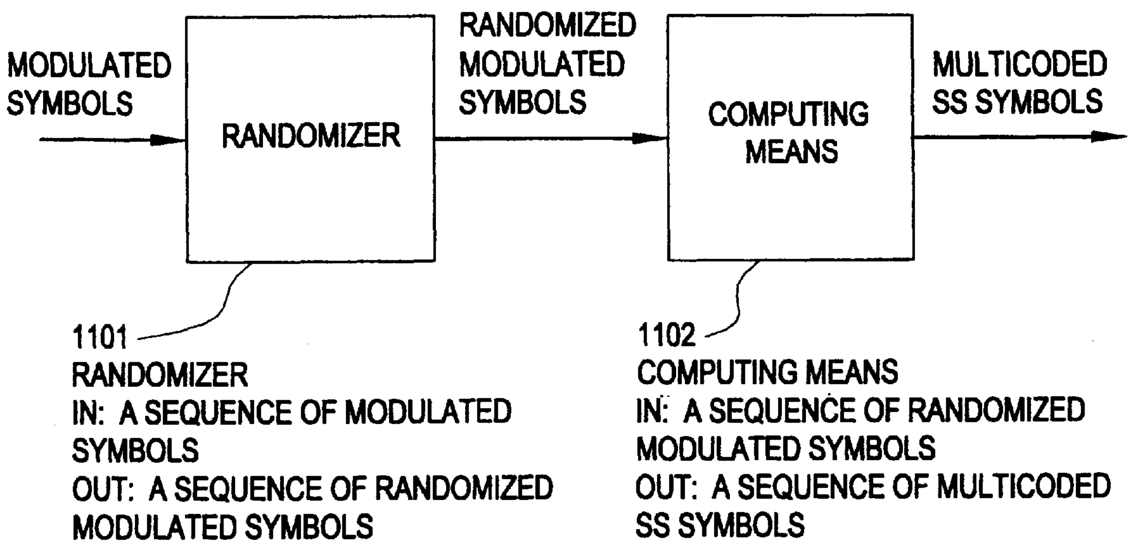

MODULATED SYMBOLS
RANDOMIZER
RANDOMIZED MODULATED SYMBOLS
COMPUTING MEANS
MULTICODED SS SYMBOLS
1101
RANDOMIZER
IN: A SEQUENCE OF MODULATED SYMBOLS
OUT: A SEQUENCE OF RANDOMIZED MODULATED SYMBOLS
1102
COMPUTING MEANS
IN: A SEQUENCE OF RANDOMIZED MODULATED SYMBOLS
OUT: A SEQUENCE OF MULTICODED SS SYMBOLS

FIG. 11

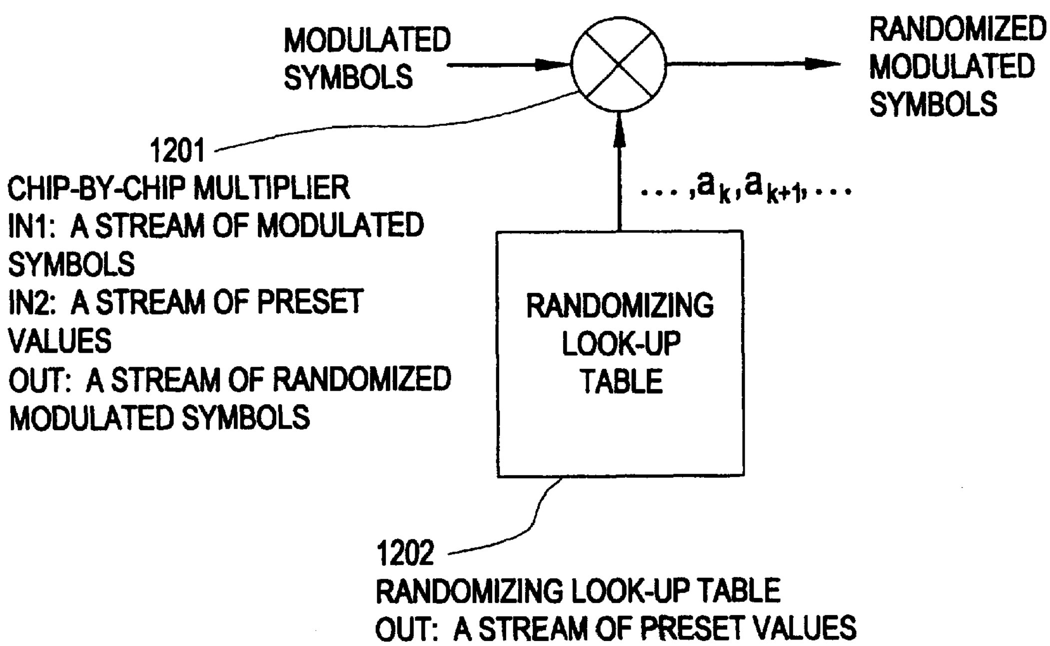

MODULATED SYMBOLS
RANDOMIZED MODULATED SYMBOLS
1201
CHIP-BY-CHIP MULTIPLIER
IN1: A STREAM OF MODULATED SYMBOLS
IN2: A STREAM OF PRESET VALUES
OUT: A STREAM OF RANDOMIZED MODULATED SYMBOLS
. . . $,a_k,a_{k+1},$ . . .
RANDOMIZING LOOK-UP TABLE
1202
RANDOMIZING LOOK-UP TABLE
OUT: A STREAM OF PRESET VALUES

FIG. 12

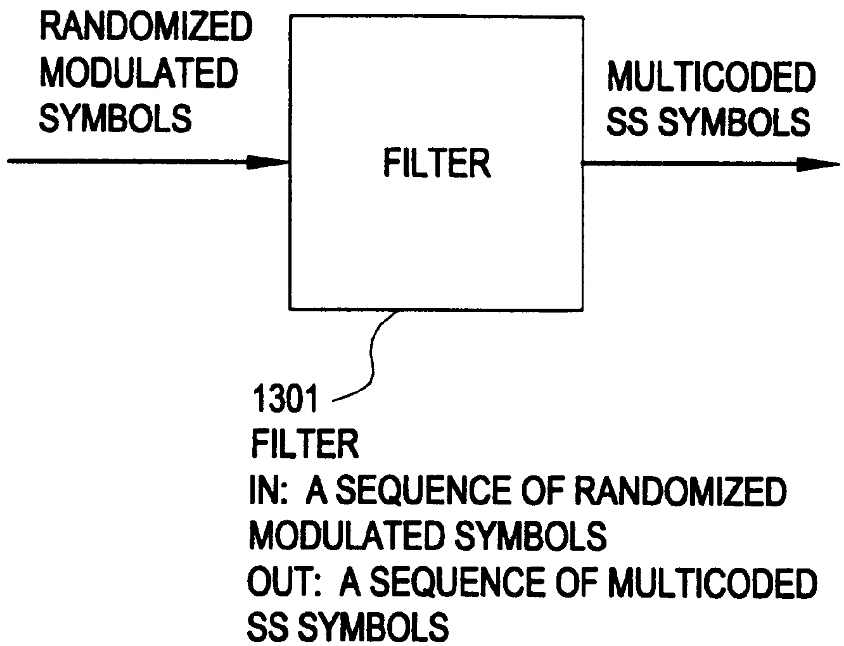

RANDOMIZED
MODULATED
SYMBOLS
FILTER
MULTICODED
SS SYMBOLS
1301
FILTER
IN: A SEQUENCE OF RANDOMIZED
MODULATED SYMBOLS
OUT: A SEQUENCE OF MULTICODED
SS SYMBOLS

FIG. 13

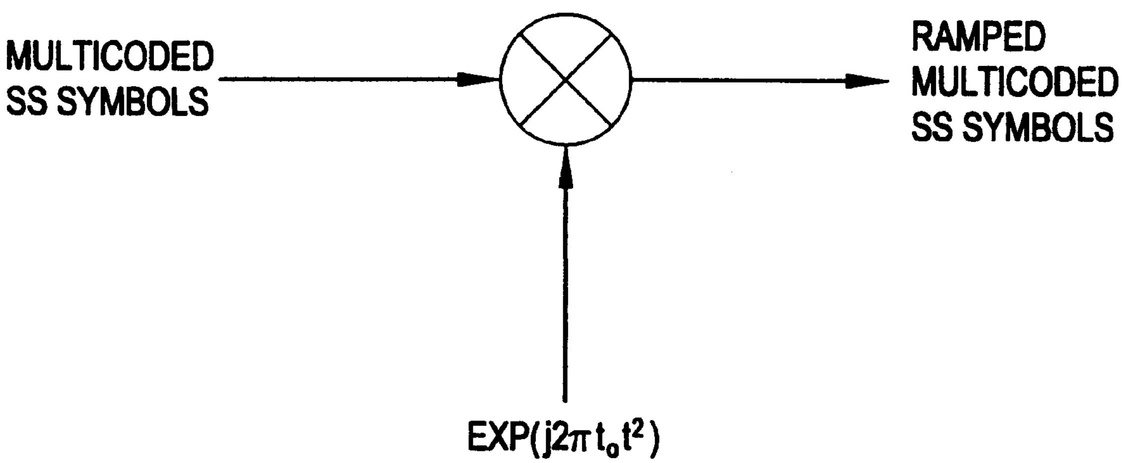

MULTICODED
SS SYMBOLS
RAMPED
MULTICODED
SS SYMBOLS
$EXP(j2\pi t_0 t^2)$

FIG. 14

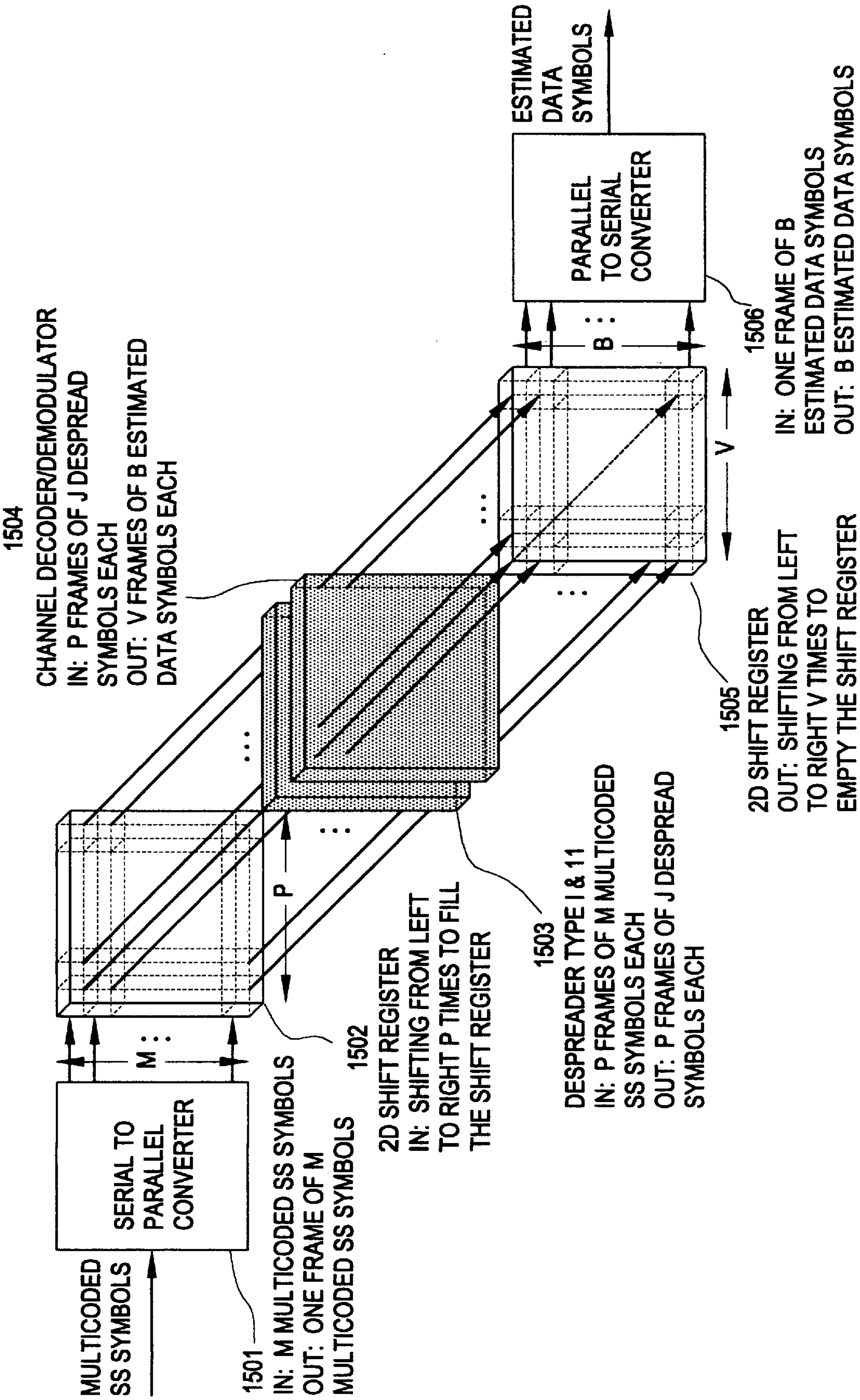

MULTICODED SS SYMBOLS
SERIAL TO PARALLEL CONVERTER
1501
IN: M MULTICODED SS SYMBOLS
OUT: ONE FRAME OF M MULTICODED SS SYMBOLS
M
1502
2D SHIFT REGISTER
IN: SHIFTING FROM LEFT TO RIGHT P TIMES TO FILL THE SHIFT REGISTER
P
1503
DESPREADER TYPE I & II
IN: P FRAMES OF M MULTICODED SS SYMBOLS EACH
OUT: P FRAMES OF J DESPREAD SYMBOLS EACH
1504
CHANNEL DECODER/DEMODULATOR
IN: P FRAMES OF J DESPREAD SYMBOLS EACH
OUT: V FRAMES OF B ESTIMATED DATA SYMBOLS EACH
1505
2D SHIFT REGISTER
OUT: SHIFTING FROM LEFT TO RIGHT V TIMES TO EMPTY THE SHIFT REGISTER
V
B
PARALLEL TO SERIAL CONVERTER
1506
IN: ONE FRAME OF B ESTIMATED DATA SYMBOLS
OUT: B ESTIMATED DATA SYMBOLS
ESTIMATED DATA SYMBOLS

FIG. 15

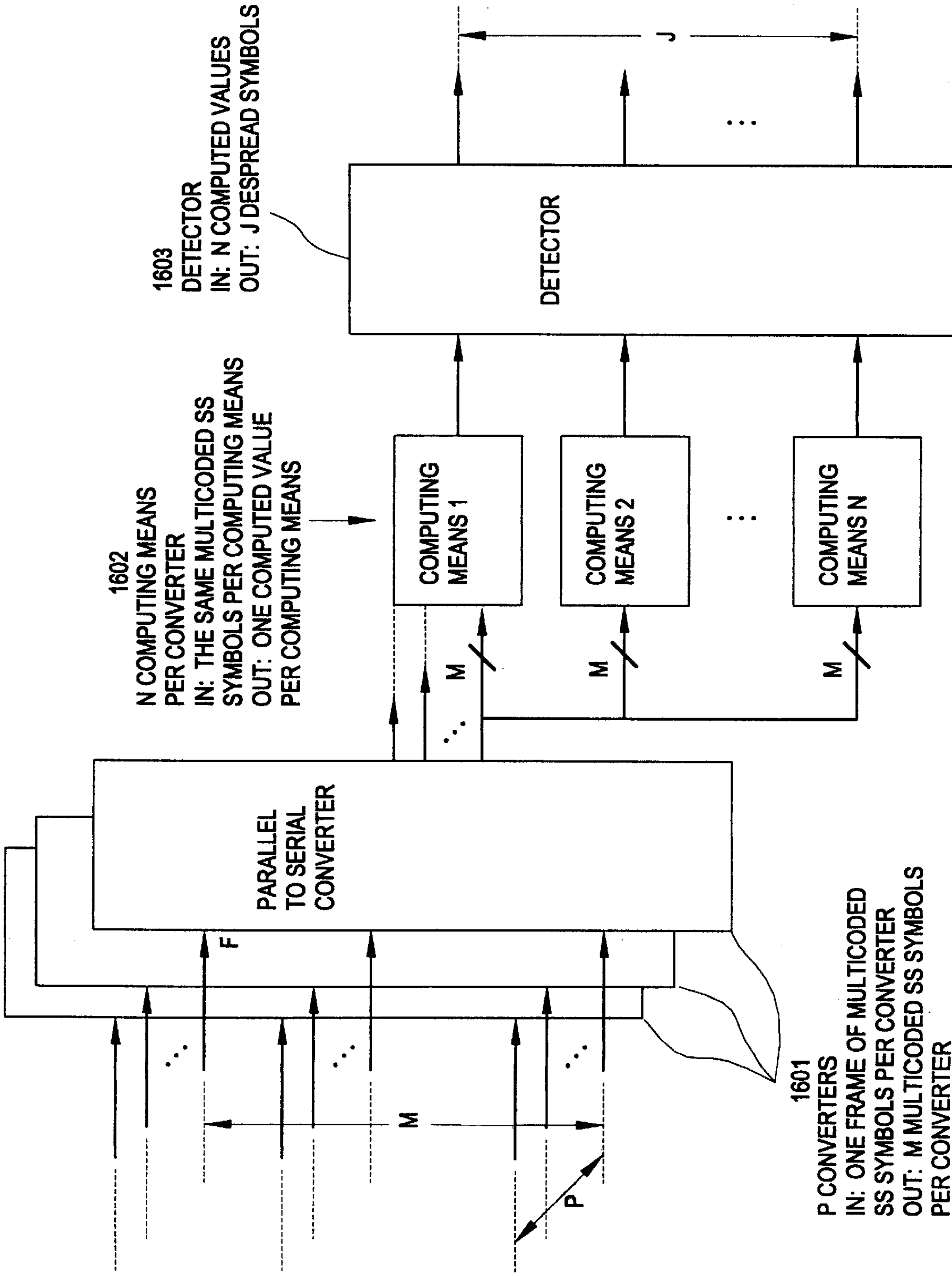
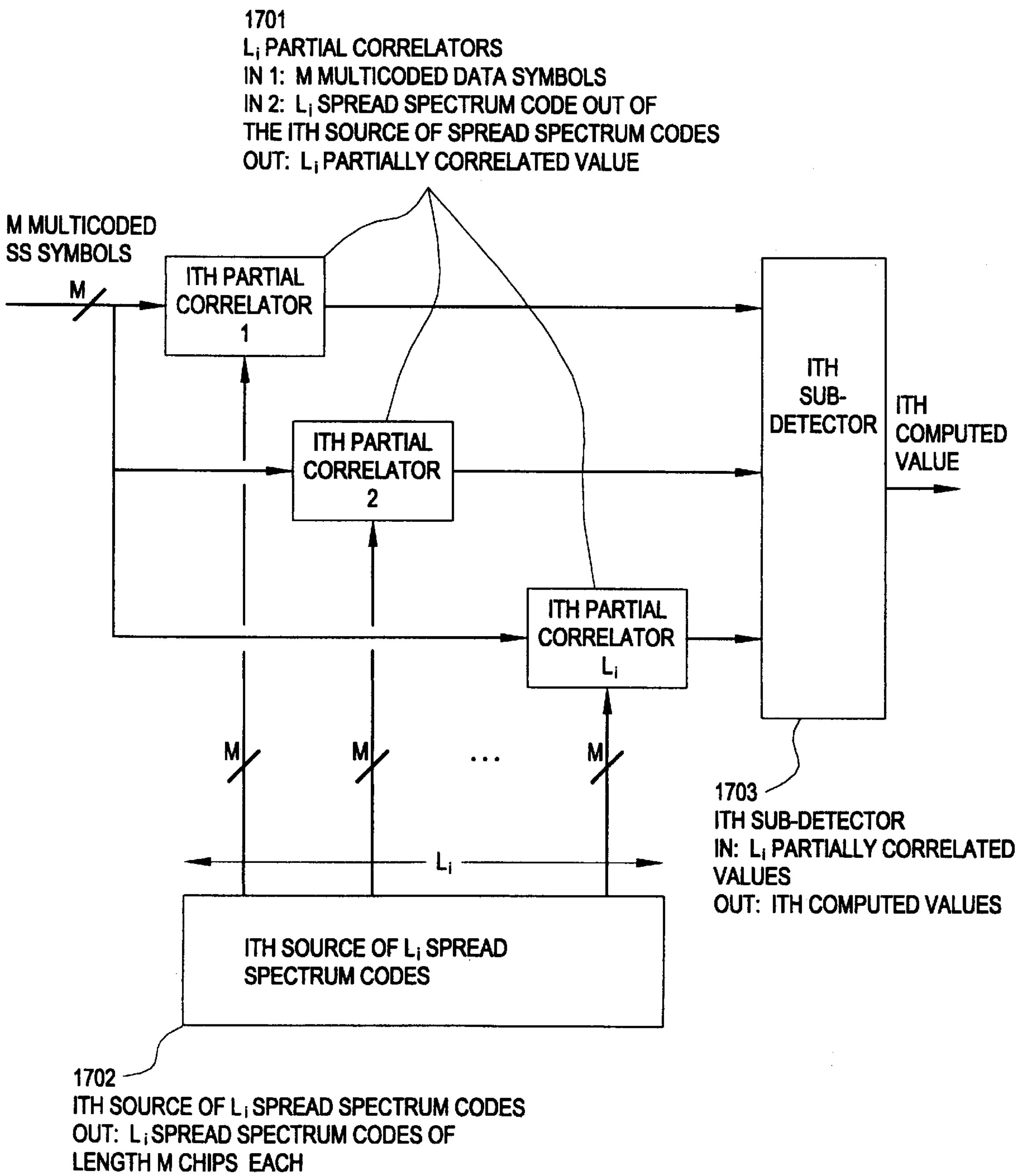

1603
DETECTOR
IN: N COMPUTED VALUES
OUT: J DESPREAD SYMBOLS
1602
N COMPUTING MEANS
PER CONVERTER
IN: THE SAME MULTICODED SS
SYMBOLS PER COMPUTING MEANS
OUT: ONE COMPUTED VALUE
PER COMPUTING MEANS
DETECTOR
J
COMPUTING
MEANS 1
COMPUTING
MEANS 2
COMPUTING
MEANS N
M
M
M
PARALLEL
TO SERIAL
CONVERTER
F
M
P
1601
P CONVERTERS
IN: ONE FRAME OF MULTICODED
SS SYMBOLS PER CONVERTER
OUT: M MULTICODED SS SYMBOLS
PER CONVERTER

FIG. 16

FIG. 17



1701
L_i PARTIAL CORRELATORS
IN 1: M MULTICODED DATA SYMBOLS
IN 2: L_i SPREAD SPECTRUM CODE OUT OF THE ITH SOURCE OF SPREAD SPECTRUM CODES
OUT: L_i PARTIALLY CORRELATED VALUE
M MULTICODED SS SYMBOLS
M
ITH PARTIAL CORRELATOR 1
ITH PARTIAL CORRELATOR 2
ITH PARTIAL CORRELATOR L_i
ITH SUB-DETECTOR
ITH COMPUTED VALUE
M
M
...
M
L_i
ITH SOURCE OF L_i SPREAD SPECTRUM CODES
1703
ITH SUB-DETECTOR
IN: L_i PARTIALLY CORRELATED VALUES
OUT: ITH COMPUTED VALUES
1702
ITH SOURCE OF L_i SPREAD SPECTRUM CODES
OUT: L_i SPREAD SPECTRUM CODES OF LENGTH M CHIPS EACH

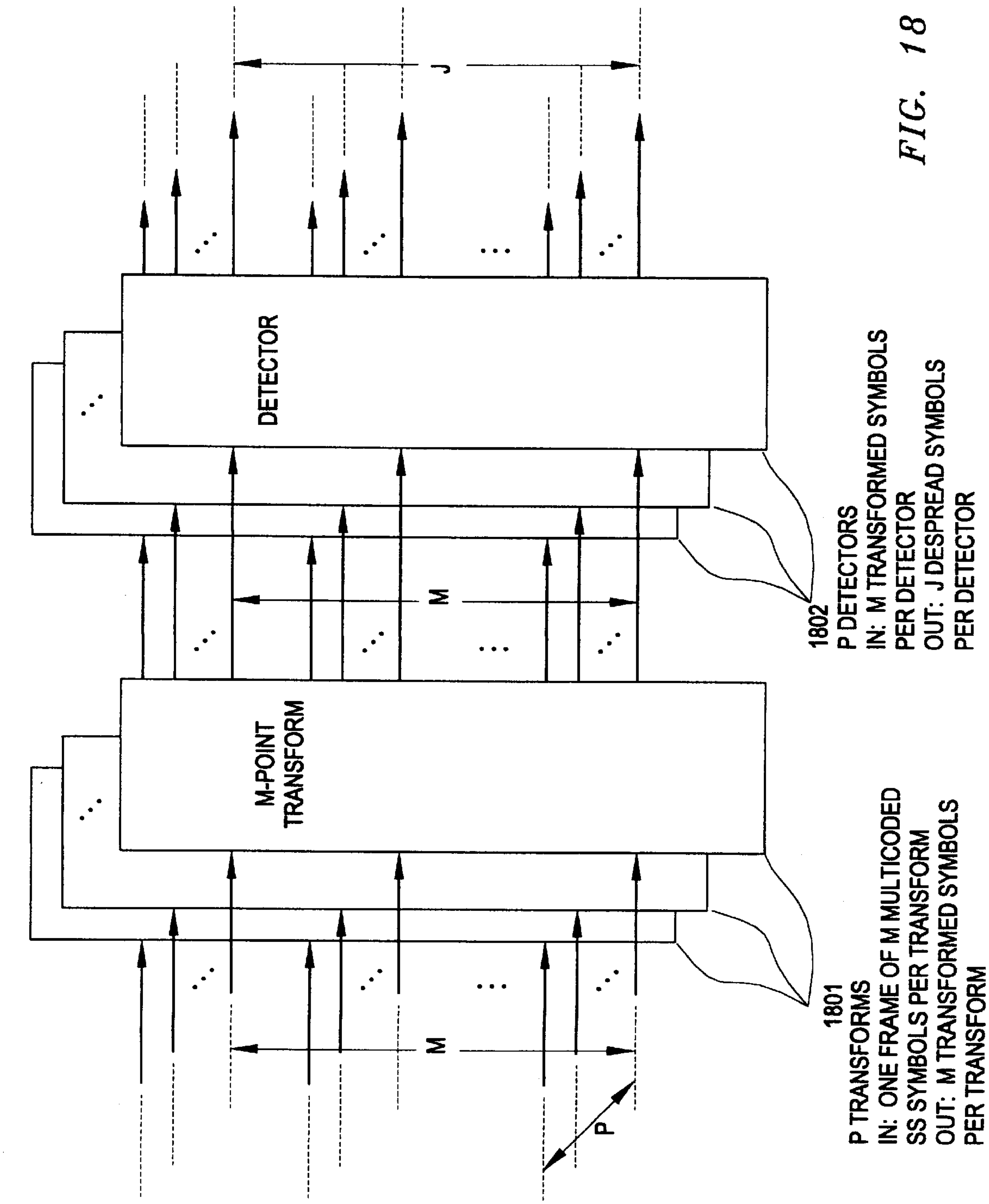

J
DETECTOR
M
1802
P DETECTORS
IN: M TRANSFORMED SYMBOLS
PER DETECTOR
OUT: J DESPREAD SYMBOLS
PER DETECTOR
M-POINT
TRANSFORM
M
P
1801
P TRANSFORMS
IN: ONE FRAME OF M MULTICODED
SS SYMBOLS PER TRANSFORM
OUT: M TRANSFORMED SYMBOLS
PER TRANSFORM

FIG. 18

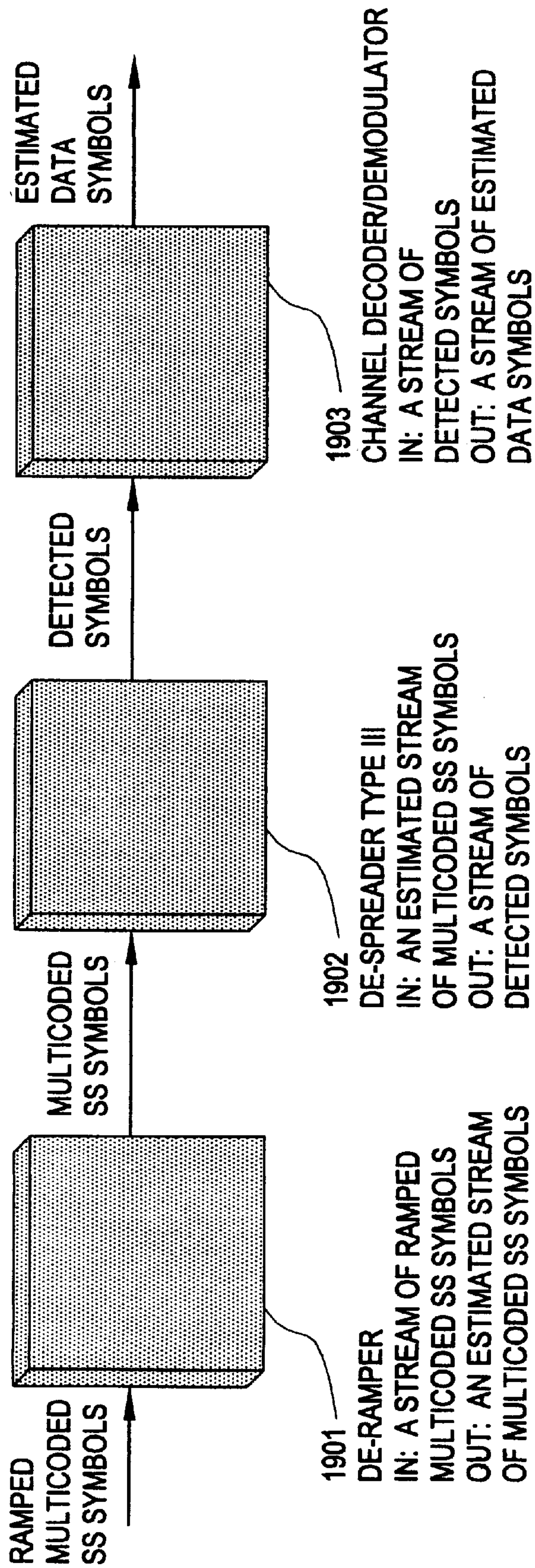

RAMPED MULTICODED SS SYMBOLS
1901
DE-RAMPER
IN: A STREAM OF RAMPED MULTICODED SS SYMBOLS
OUT: AN ESTIMATED STREAM OF MULTICODED SS SYMBOLS
MULTICODED SS SYMBOLS
1902
DE-SPREADER TYPE III
IN: AN ESTIMATED STREAM OF MULTICODED SS SYMBOLS
OUT: A STREAM OF DETECTED SYMBOLS
DETECTED SYMBOLS
1903
CHANNEL DECODER/DEMODULATOR
IN: A STREAM OF DETECTED SYMBOLS
OUT: A STREAM OF ESTIMATED DATA SYMBOLS
ESTIMATED DATA SYMBOLS

FIG. 19

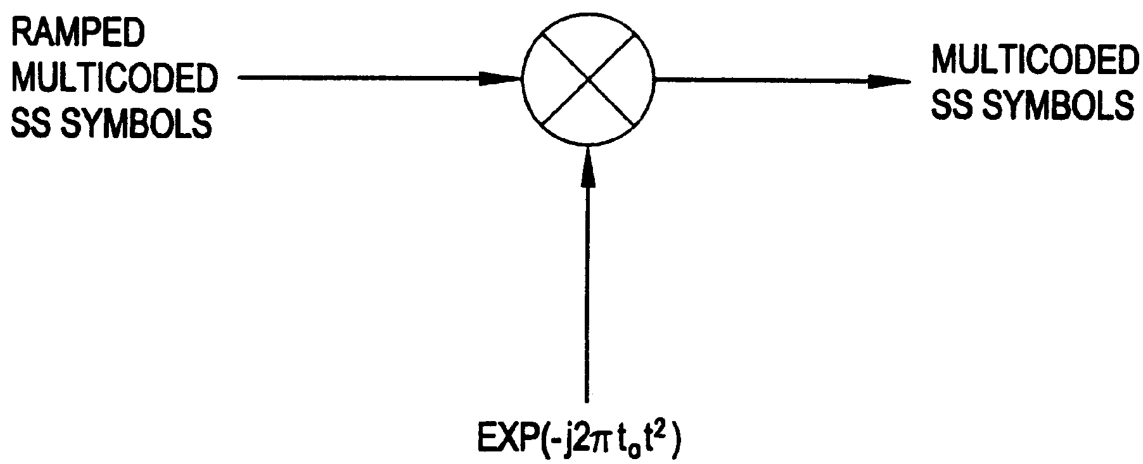

RAMPED
MULTICODED
SS SYMBOLS
MULTICODED
SS SYMBOLS
EXP(-j2π t₀t²)

FIG. 20

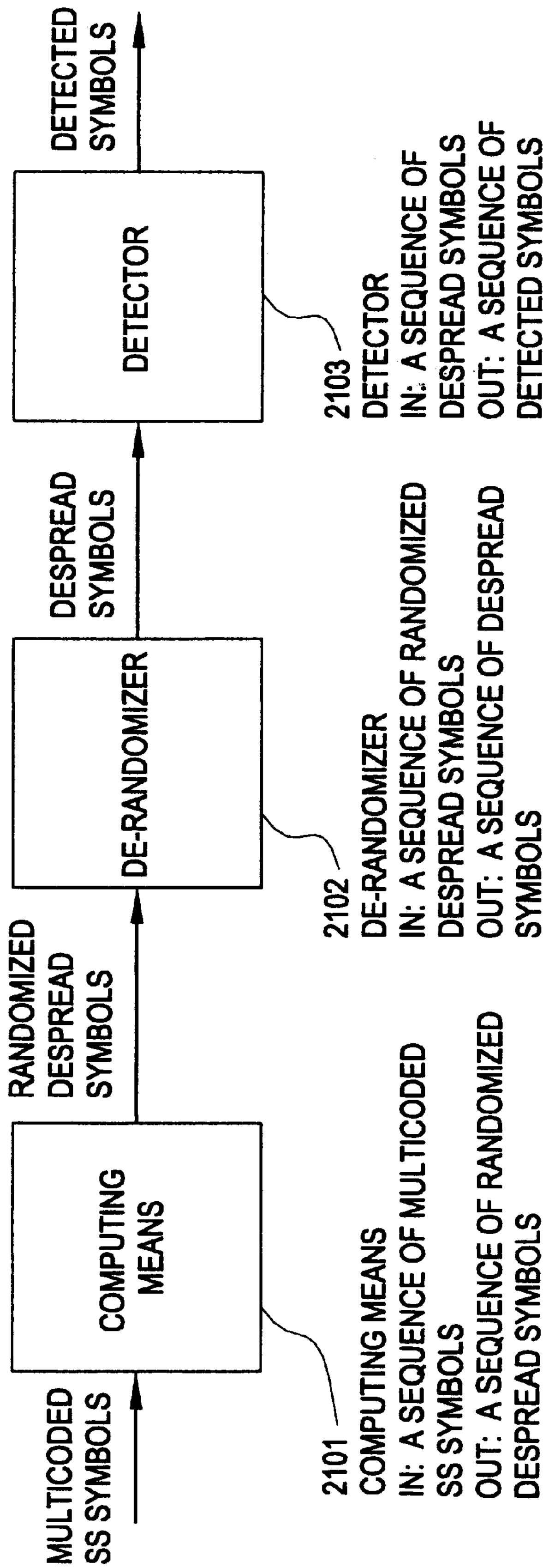

MULTICODED SS SYMBOLS
COMPUTING MEANS
RANDOMIZED DESPREAD SYMBOLS
DE-RANDOMIZER
DESPREAD SYMBOLS
DETECTOR
DETECTED SYMBOLS
2101
COMPUTING MEANS
IN: A SEQUENCE OF MULTICODED SS SYMBOLS
OUT: A SEQUENCE OF RANDOMIZED DESPREAD SYMBOLS
2102
DE-RANDOMIZER
IN: A SEQUENCE OF RANDOMIZED DESPREAD SYMBOLS
OUT: A SEQUENCE OF DESPREAD SYMBOLS
2103
DETECTOR
IN: A SEQUENCE OF DESPREAD SYMBOLS
OUT: A SEQUENCE OF DETECTED SYMBOLS

FIG. 21

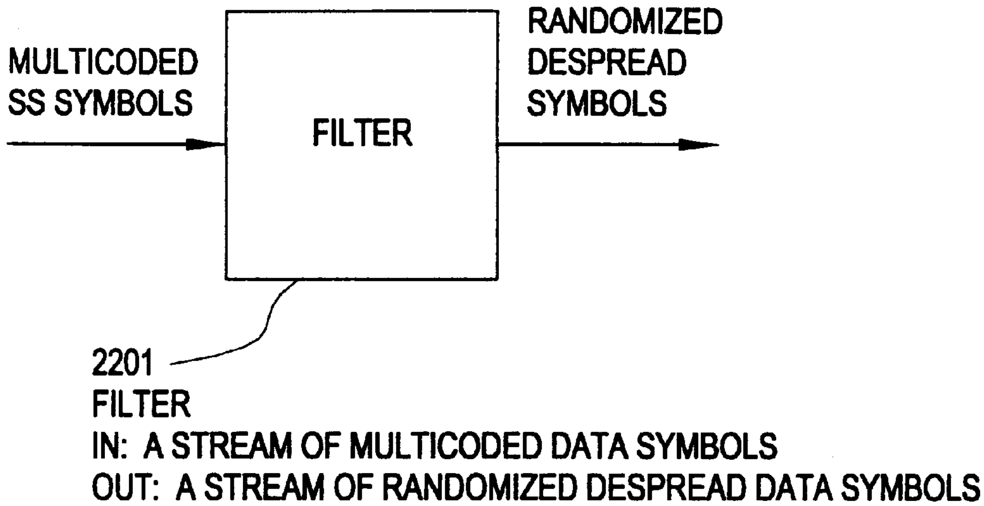

MULTICODED
SS SYMBOLS
FILTER
RANDOMIZED
DESPREAD
SYMBOLS
2201
FILTER
IN: A STREAM OF MULTICODED DATA SYMBOLS
OUT: A STREAM OF RANDOMIZED DESPREAD DATA SYMBOLS

FIG. 22

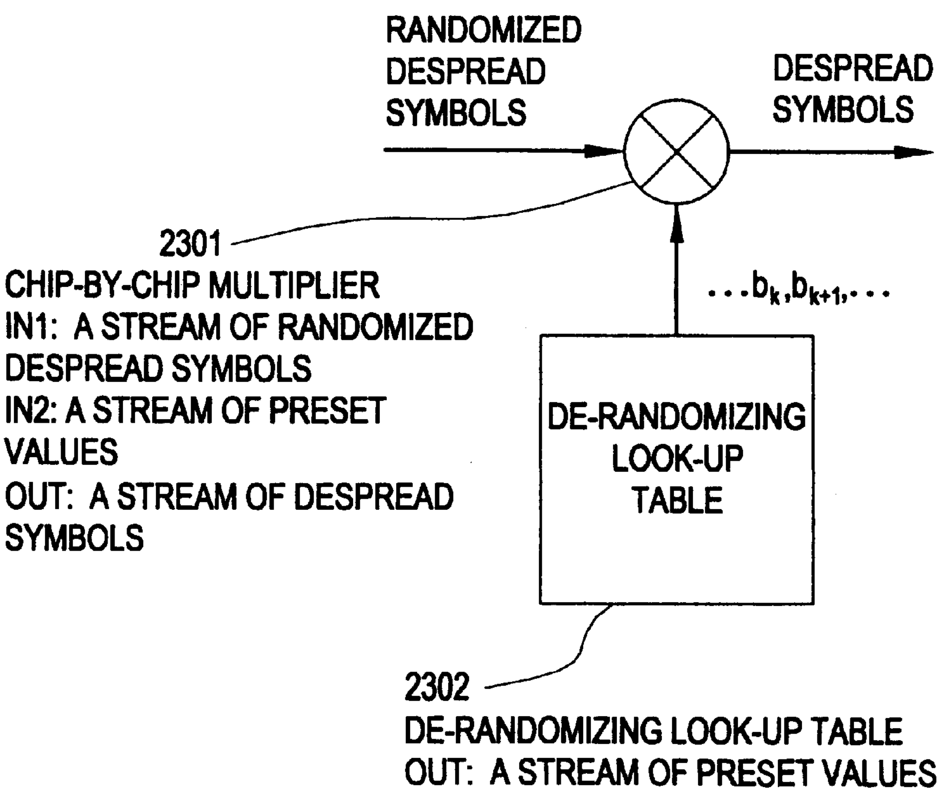

RANDOMIZED
DESPREAD
SYMBOLS
DESPREAD
SYMBOLS
2301
CHIP-BY-CHIP MULTIPLIER
IN1: A STREAM OF RANDOMIZED
DESPREAD SYMBOLS
IN2: A STREAM OF PRESET
VALUES
OUT: A STREAM OF DESPREAD
SYMBOLS
...b_k,b_{k+1},...
DE-RANDOMIZING
LOOK-UP
TABLE
2302
DE-RANDOMIZING LOOK-UP TABLE
OUT: A STREAM OF PRESET VALUES

FIG. 23

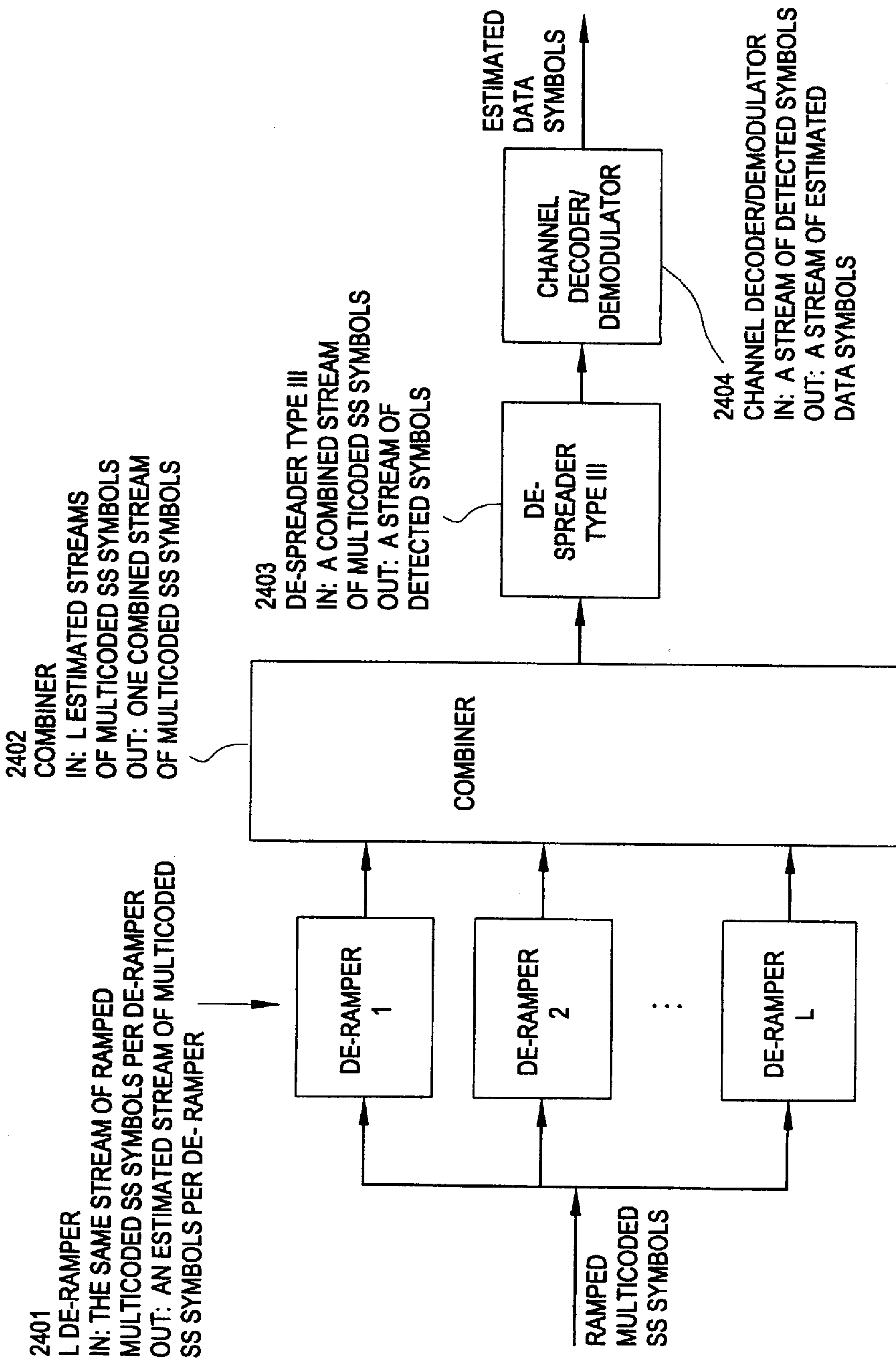

2401
L DE-RAMPER
IN: THE SAME STREAM OF RAMPED MULTICODED SS SYMBOLS PER DE-RAMPER
OUT: AN ESTIMATED STREAM OF MULTICODED SS SYMBOLS PER DE-RAMPER
2402
COMBINER
IN: L ESTIMATED STREAMS OF MULTICODED SS SYMBOLS
OUT: ONE COMBINED STREAM OF MULTICODED SS SYMBOLS
2403
DE-SPREADER TYPE III
IN: A COMBINED STREAM OF MULTICODED SS SYMBOLS
OUT: A STREAM OF DETECTED SYMBOLS
2404
CHANNEL DECODER/DEMODULATOR
IN: A STREAM OF DETECTED SYMBOLS
OUT: A STREAM OF ESTIMATED DATA SYMBOLS
RAMPED MULTICODED SS SYMBOLS
DE-RAMPER 1
DE-RAMPER 2
...
DE-RAMPER L
COMBINER
DE-SPREADER TYPE III
CHANNEL DECODER/ DEMODULATOR
ESTIMATED DATA SYMBOLS

FIG. 24

MULTICODE SPREAD SPECTRUM COMMUNICATIONS SYSTEM

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. application Ser. No. 08/725,556, filed on Oct. 3, 1996, now U.S. Pat. No. 6,192,068, priority from the filing date of which is hereby claimed under 35 U.S.C. §120.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

Not applicable.

FIELD OF THE INVENTION

The invention deals with the field of multiple access communications using Spread Spectrum modulation. Multiple access can be classified as either random access, polling, TDMA, FDMA, CDMA or any combination thereof. Spread Spectrum can be classified as Direct Sequence, Frequency-Hopping or a combination of the two.

BACKGROUND OF THE INVENTION

Commonly used spread spectrum techniques are Direct Sequence Spread Spectrum (DSSS) and Code Division Multiple Access (CDMA) as explained respectively in Chapters 13 and 15 of "Digital Communication" by J. G. Proakis, Third Edition, 1995, McGraw Hill. DSSS (See Simon M. K. et al., "Spread Spectrum Communications Handbook," Revised Edition, McGraw-Hill, 1994 and see Dixon, R. C., "Spread Spectrum systems with commercial applications," Wiley InterScience, 1994) is a communication scheme in which information symbols are spread over code bits (generally called chips). It is customary to use noise-like codes called pseudo-random noise (PN) sequences. These PN sequences have the property that their auto-correlation is almost a delta function. In other words, proper codes perform an invertible randomized spreading of the information sequence. The advantages of this information spreading are:

1. The transmitted signal can be buried in noise and thus has a low probability of intercept.
2. The receiver can recover the signal from interferers (such as other transmitted codes) with a jamming margin that is proportional to the spreading code length.
3. DSSS codes of duration longer than the delay spread of the propagation channel can lead to multipath diversity implementable using a Rake receiver.
4. The FCC and Industry Canada have allowed the use of unlicensed low power DSSS systems of code lengths greater than or equal to 10 (part 15 rules) in some frequency bands (the ISM bands).

It is the last advantage (i.e. advantage 4, above) that has given much interest recently to DSSS.

An obvious limitation of DSSS systems is the limited throughput they can offer. In any given bandwidth, W, a code of length M will reduce the effective bandwidth to W/M. To increase the overall bandwidth efficiency, system designers introduced Code Division Multiple Access (CDMA) where multiple DSSS communication links can be established simultaneously over the same frequency band provided each link uses a unique code that is noise-like, i.e. provided the cross-correlation between codes is almost null. Examples of CDMA is the next generation of digital Cellular communications in North America: "the TIA Interim Standard IS-95," (see QUALCOMM Inc., "An overview of the application of Code Division Multiple Access (CDMA) to digital cellular systems and personal cellular networks," May 21, 1992 and see Viterbi, A. J., "CDMA, Principles of Spread Spectrum Communications," Addison-Wesley, 1995) where a Base Station (BS) communicates to a number of Mobile Stations (MS) simultaneously over the same channel. The MSs share one carrier frequency during the mobile-to-base link (also known as the reverse link) which is 45 MHz away from the one used by the BS during the base-to-mobile link (also known as the forward link). During the forward link, the BS transceiver is assigned N codes where N is less than or equal to M and M is the number of chips per DSSS code. During the reverse link each MS is assigned a unique code.

CDMA problems are:

1. The near-far problem on the reverse link: an MS transmitter "near" the BS receiver can overwhelm the reception of codes transmitted from other MSs that are "far" from the BS.
2. Synchronization on the reverse link: synchronization is complex (especially) if the BS receiver does not know in advance either the identity of the code being transmitted, or its time of arrival.

SUMMARY OF THE INVENTION

We have recognized that low power DSSS systems would be ideal communicators provided the problems of CDMA could be resolved. In order to avoid both the near-far problem and the synchronization problem that exist on the reverse link of a CDMA system, we have opted in this patent to use only the forward link at all times for MCSS Types I and II. This is achieved within a specified channel by allowing only one transceiver to transmit at a time within a certain coverage area. Such a transceiver is forced during transmission to act as the BS in transmit mode while the remaining transceivers are forced to act as MSs in receive mode. In this patent, we refer to such a modulation scheme as MultiCode Spread Spectrum (MCSS).

On the other hand, both the near-far problem and the synchronization problem that exist on the reverse link of a CDMA system are reduced drastically by using MCSS Type III. In this case, each user is assigned one code and each code is assigned a guard time such that it starts to transmit only after a given amount of time relative to any adjacent codes. By forcing the users to have separate start times, MCSS Type III forces the codes to be (quasi) orthogonal as long as the guard time between adjacent codes is long enough.

When viewed as DSSS, a MCSS receiver requires up to N correlators (or equivalently up to N Matched Filters) (such as in QUALCOMM Inc,. "An overview of the application of Code Division Multiple Access (CDMA)" to digital cellular systems and personal cellular networks, May 21, 1994 and as in Viterbi, A. J., "CDMA, Principles of Spread Spectrum Communications," Addison-Wesley, 1995) with a complexity of the order of NM operations. When both N and M are large, this complexity is prohibitive. In addition, a nonideal communication channel can cause InterCode Interference (ICI), i.e. interference between the N SS codes at the receiver. In this patent, we introduce three new types of MCSS. MCSS Type I allows the information in a MCSS signal to be detected using a sequence of partial correlations with a combined complexity of the order of M operations. MCSS Type II allows the information in a MCSS signal to be detected in a sequence of low complexity parallel operations while reducing the ICI. MCSS Type III allows the information in a MCSS signal to be detected in a sequence of low complexity Multiply and Accumulate (MAC) opera-

tions implementable as a filter, which reduce the effect of multipath. In addition to low complexity detection and ICI reduction, our implementation of MCSS has the advantage that it is spectrally efficient since N can be made approximately equal to M. In DSSS, N=1 while in CDMA typically N<0.4M.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated and better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIG. **1** provides an illustration of a Transmitter for MCSS Type I, wherein VB data symbols in VBT seconds are input and PM multicoded SS symbols in PMT_C seconds are output;

FIG. **2** provides a schematic illustration of a Spreader Type I (**104**) from FIG. **1**, in which P frames of J modulated symbols each are input and P frames of N spread spectrum symbols each, of length M chips per spread spectrum symbol are output;

FIG. **3** provides a schematic of the ith computing means (**202**) from FIG. **2**, in which an ith subset of modulated symbols is input and an ith spread spectrum symbol of length M chips is output;

FIG. **4** provides a schematic of the ith source (**302**) from FIG. **3** of L_i spread spectrum codes, in which L_i preset sequences of length M chips each are input, and L_i spread spectrum codes of length M chips each are output;

FIG. **5** provides a schematic of the ith source (**302**) from FIG. **3** of L_i spread spectrum codes, in which L_i preset values of length M chips each are input, and L_i spread spectrum codes of length M chips each are output;

FIG. **6** provides a schematic of the Transmitter for MCSS Type II, in which VB data symbols in VBT seconds are input, and PM multicoded SS symbols in PMT_C seconds are output;

FIG. **7** provides a schematic of the Spreader Type II (**604**) from FIG. **6**, in which P frames of J modulated symbols each are input and P frames of M multicoded SS symbols are output;

FIG. **8** provides the ith M-point Transform (**702**) from FIG. **7**, in which M subsets of modulated symbols are input and M multicoded SS symbols are output;

FIG. **9** provides the ith M-point Transform (**702**) from FIG. **7**, in which M subsets of modulated symbols are input and M multicoded SS symbols are output;

FIG. **10** provides a schematic of the MCSS Transmitter Type III, in which a stream of data symbols is input and a stream of ramped multicoded SS symbols is output;

FIG. **11** provides a schematic of the Spreader (**1002**) Type III in FIG. **10**, in which a sequence of modulated symbols is input and a sequence of multicoded SS symbols is output;

FIG. **12** provides a schematic of the Randomizer (**1101**) in FIG. **11**, in which a sequence of modulated symbols is input and a sequence of randomized modulated symbols is output;

FIG. **13** provides a schematic of the Computing Means (**1102**) in FIG. **11**, in which a sequence of randomized modulated symbols is input and a sequence of multicoded SS symbols is output;

FIG. **14** provides a schematic of the Ramper (**1003**) in FIG. **10** for ramping the multicoded SS symbols using a linearly ramping carrier frequency, in which a sequence of multicoded SS symbols is input and a sequence of ramped multicoded SS symbols is output;

FIG. **15** provides a schematic of the Receiver for MCSS Type I & II, in which PM multicoded SS symbols in PMT_C seconds is input and VB estimated data symbols in VBT seconds is output;

FIG. **16** provides a schematic of the Despreader Type I (**1503**) from FIG. **15**, in which P frames of M multicoded SS symbols each are input and P frames of J despread symbols each is output;

FIG. **17** provides a schematic of the ith computing means (**1602**) from FIG. **16**, in which M multicoded SS symbols are input and ith computed values are output;

FIG. **18** provides a schematic of the Despreader Type II (**1503**) from FIG. **15**, in which P frames of M multicoded SS symbols each are input and P frames of J despread symbols each are output;

FIG. **19** provides a schematic of the Receiver for MCSS Type III, in which a stream of multicoded SS symbols are input and a stream of estimated data symbols are output;

FIG. **20** provides the De-ramper (**1901**) in FIG. **19** for de-ramping the ramped milticoded SS symbols using a linearly de-ramping carrier frequency, in which a stream of ramped multicoded SS symbols are input and an estimated stream of multicoded SS symbols are output;

FIG. **21** provides a schematic of the De-Spreader (**1902**) Type III in FIG. **19**, in which a sequence of multicoded SS symbols is input and a sequence of detected symbols is output;

FIG. **22** provides a schematic of the computing means (**2101**) in FIG. **21**, in which a stream of multicoded SS symbols is input and a stream of randomized despread symbols is output;

FIG. **23** provides a schematic of the De-Randomizer (**2102**) in FIG. **21**, in which a sequence of randomized despread data symbols is input and a sequence of despread symbols is output; and

FIG. **24** provides a preferred diversity receiver for MCSS Type III with de-ramping, in which a stream of ramped multicoded SS symbols is input and a stream of estimated data symbols is output.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The description of the invention consists of six parts. The first three parts correspond to the transmitter for each one of the three types of MCSS introduced in this patent, while the last three parts correspond to the receiver for each one of the three types of MCSS.

Description of the Transmitter for MCSS Type I

FIG. **1** illustrates a block diagram of the transmitter for MCSS Type I with an input of V frames of B data symbols each, every VBT seconds and an output of P frames of M multicoded SS symbols each, every PMT_C seconds where T is the duration of one data symbol and T_C is the duration of one chip in a spread spectrum code. The data symbols can be either analog or digital. If digital, they belong to an alphabet of finite size. If analog, they correspond to the samples of an analog signal.

FIG. **1** is described as follows:

- The first block in FIG. **1** is a serial-to-parallel converter (**101**) with an input of B data symbols and an output of one frame of B data symbols, every BT seconds.
- The second block is a 2 Dimensional (2D) shift register (**102**) with an input of V frames of B data symbols each

(input by shifting the frames from left to right V times) and an output of Q frames of B data symbols each, every VBT seconds.

When the data symbols are analog, the third block (**103**) in FIG. **1** corresponds to an analog pulse modulator with several possible modulation schemes such as Pulse Amplitude Modulation (PAM), Pulse Position Modulation (PPM), Pulse Frequency Modulation (PFM), etc. When the data symbols are digital, the third block is a channel encoder/modulator (**103**) with an input of Q frames of B data symbols each and an output of P frames of J modulated symbols each, every QBT seconds. The channel encoder/modulator performs two functions: (1) to encode and (2) to modulate the data symbols. The first function offers protection to the symbols against a non ideal communication channel by adding redundancy to the input sequence of data symbols while the second function maps the protected symbols into constellation points that are appropriate to the communication channel. Sometimes it is possible to perform the two functions simultaneously such as in the case of Trellis Coded Modulation (TCM). For simplicity, we assume throughout the patent that the two functions are performed simultaneously and refer to the block performing the two functions as the channel encoder/modulator.

Different types of channel encoders are available:

If the 2D shift register (**102**) is operated with: V=Q, then the encoder performs block encoding, otherwise if V<Q, the encoder performs convolutional encoding. Furthermore, if B>J then the encoder is a trellis encoded modulator either with block encoding if V=Q or with convolutional encoding with V<Q.

If B=J, the code rate is Q/P, i.e. the encoder takes Q data symbols in and generates P encoded data symbols out where P>Q. Furthermore, if V<Q then (V−1) is the constraint length of the convolutional encoder.

If the 2D shift register (**102**) is operated with B>1, then it can act as an interleaver which interleaves the data symbols prior to the channel encoder (**103**), otherwise if B=1 the channel encoder does not rely on interleaving. Another possible form of interleaving is to interleave the coded data symbols after the channel encoder (not shown in FIG. **1**).

Different types of modulators are available such as: Binary Phase Shift Keying (BPSK), Quadrature Phase Shift Keying (QPSK), Multilevel Phase Shift Keying (MPSK), Quadrature Amplitude Modulation (QAM), Frequency Shift Keying (FSK), Continuous Phase Modulation (CPM), Amplitude Shift Keying (ASK), etc. All amplitude and frequency modulation schemes can be demodulated either coherently or noncoherently. All phase modulation schemes can de demodulated either coherently or differentially. In the latter case, differential encoding is required in the modulator such as in Differential BPSK (DBPSK), Differential QPSK (DQPSK), Differential MPSK (DMPSK), etc. Even though the output of the channel encoder/modulator (**103**) corresponds to an encoded and modulated data symbol, we will refer to it of as a ‘modulated symbol’.

The fourth block is a spreader type I (**104**) with an input of P frames of J modulated symbols each and an output of P frames of N spread spectrum symbols each, of length M chips per spread spectrum symbol, every PMT_C seconds. The spreader type I (**104**) is explained further below in FIGS. **2**–**5**.

The fifth block is a 3 Dimensional (3D) shift register (**105**) with an input of P frames of N spread spectrum symbols each (input by shifting the PN symbols from inside to outside M chip times), and an output of M frames of N chips each (output by shifting MN chips from left to right P times) every PMT_C seconds.

The sixth block is a set of M adders (**106**). Each adder has an input of N chips and an output of one multicoded SS symbol, every MT_C seconds.

The seventh block is a parallel-to-serial converter (**107**) with an input of one frame of M multicoded SS symbol and an output of M multicoded SS symbol every MT_C seconds.

The spreader type I (**104**) in FIG. **1** is described further in FIG. **2** with an input of P frames of J modulated symbols each, generated by the channel encoder/modulator (**103**) in FIG. **1**, and an output of P frames of N spread spectrum symbols each, of length M chips per spread spectrum symbol. FIG. **2** is described as follows:

The first block in FIG. **2** is a set of P converters (**201**) with an input of one frame of J modulated symbols per converter, and an output of one frame of N subsets of modulated symbols per converter. The ith subset contains a number J_i of modulated symbols where $J_1+J_2+\ldots+J_N=J$ and i=1, . . . ,N.

The second block is a set of N computing means (**202**) with an input of one subset of modulated symbols per computing means, and an output of one spread spectrum symbol, of length M chips per computing means.

The set of N computing means (**202**) in FIG. **2** is described further in FIG. **3** which displays only the ith computing mean where i=1, . . . ,N. The ith computing mean has as an input the ith subset of modulated symbols, and as an output the ith spread spectrum symbol of length M chips. FIG. **3** is described as follows.

The first block in FIG. **3** is the ith mapper (**301**) with two inputs and one output. The two inputs are: (1) the ith subset of modulated symbols which contains a number J_i of modulated symbols, and (2) L_i spread spectrum codes of length M chips each. The output is the ith spread spectrum symbol. The ith mapper chooses from the set of L_i spread spectrum codes the code corresponding to the ith subset of modulated symbols to become the ith spread spectrum code representing an invertible randomized spreading of the ith subset of modulated symbols.

The second block in FIG. **3** is the ith source (**302**) of L_i spread spectrum codes with an output of L_i spread spectrum codes of length M chips each. The ith source (**302**) can be thought of as either a lookup table or a code generator. Two different implementations of the ith source are shown in FIGS. **4** and **5**.

Remarks on the “Invertible Randomized Spreading”

1. In this patent, the invertible randomized spreading of a signal using a spreader is only invertible to the extent of the available arithmetic precision of the machine used to implement the spreader. In other words, with finite precision arithmetic, the spreading is allowed to add a limited amount of quantization noise.
2. Moreover, the randomized spreading of a signal is not a perfect randomization of the signal (which is impossible) but only a pseudo-randomization. This is typical of spread spectrum techniques in general.
3. Finally, in some cases such as over the multipath communication channel, it is advantageous to spread the signal over a bandwidth wider than 25% of the coherence bandwidth of the channel. In this patent, we refer to such a spreading as wideband spreading. In the indoor wireless

channel, 25% of the coherence bandwidth ranges from 2 MHz to 4 MHz. In the outdoor wireless channel, 25% of the coherence bandwidth ranges from 30 KHz to 60 KHz. In other words, in this patent wideband spreading corresponds to a spreading of the information signal over a bandwidth wider than 30 KHz over the outdoor wireless channel and wider than 2 MHz over the indoor wireless channel, regardless of the bandwidth of the information signal and regardless of the carrier frequency of modulation.

The ith source **(302)** of FIG. **3** can also be generated as in FIG. **4** as a set of L_i transforms with an input of one preset sequence of length M chips per transform and an output of one spread spectrum code of length M chips per transform. In other words, the ith source of spread spectrum codes could be either a look-up table containing the codes such as in FIG. **3** or a number of transforms generating the codes such as in FIG. **4**.

The ith source **(302)** of FIG. **3** can also be generated as in FIG. **5** as two separate blocks.

The first block **(501)** consists of a set of L_i transforms with an input of one preset sequence of length M chips per transform and an output of one spread spectrum code of length M chips per transform.

The second block is a randomizing transform **(502)** with an input of L_i transformed codes of length M chips each generated by the first block **(501)** and an output of L_i spread spectrum codes of length M chips each.

The randomizing transform consists of two parts. The first part is a randomizing look-up table **(503)** which contains a set of M preset values: $a_{1,i}$, $a_{2,i}$, . . . ,$a_{M,i}$. The second part multiplies each transformed symbol from the set of transformed symbols generated by the first transform **(501)** by the set of M preset values generated by the randomizing look-up table **(503)**. The multiplication is performed chip-by-chip, i.e. the kth chip in the ith transformed symbol is multiplied by the kth value $a_{k,i}$ in the set of M preset values for all values of k=1, . . . , M.

Description of the Transmitter for MCSS Type II

FIG. **6** illustrates a block diagram of the transmitter for MCSS Type II with an input of VB data symbols every VBT seconds and an output of PM multicoded SS symbols every PMT_C seconds. FIG. **6** is described as follows:

The first block in FIG. **6** is a serial-to-parallel converter **(601)** with an input of B data symbols and an output of one frame of B data symbols, every BT seconds.

The second block is a 2 Dimensional (2D) shift register **(602)** with an input of V frames of B data symbols each (input by shifting the frames from left to right V times) and an output of Q frames of B data symbols each, every VBT seconds.

The third block is a channel encoder/modulator **(603)** with an input of Q frames of B data symbols each and an output of P frames of J modulated symbols each, every QBT seconds. The function of the channel encoder/modulator is exactly the same as the channel encoder/modulator **(103)** described above for MCSS type I in FIG. **1**.

The fourth block is a spreader type II **(604)** with an input of P frames of J modulated symbols each and an output of P frames of M multicoded SS symbols each, every PMT_C seconds. The spreader type II is explained further below in FIGS. **7–9**.

The fifth block is a 2 Dimensional (2D) shift register **(605)** with an input of P frames of M multicoded SS symbols each, and an output of P frames of M multicoded SS symbols each (output by shifting the M frames from left to right P times) every PMT_C seconds.

The sixth block is a parallel-to-serial converter **(606)** with an input of one frame of M multicoded SS symbols and an output of M multicoded SS symbols every MT_C seconds.

The spreader type II **(604)** in FIG. **6** is described further in FIG. **7** with an input of P frames of J modulated symbols each, generated by the channel encoder/modulator **(603)** in FIG. **6**, and an output of P frames of M multicoded SS symbols each. FIG. **7** is described as follows:

The first block in FIG. **7** is a set of P converters **(701)** with an input of one frame of J modulated symbols per converter, and an output of one frame of M subsets of modulated symbols per converter. The ith subset contains a number of J_i of modulated symbols where $J_1+J_2+ . . . +J_M=J$ and i=1, . . . ,M.

The second block is a set of P M-point transforms **(702)** with an input of M subsets of modulated symbols per transform, and an output of a frame of M multicoded SS symbols per transform. The P M-point transforms perform the invertible randomized spreading of the M subsets of modulated symbols.

The set of P M-point transforms **(702)** in FIG. **7** is described further in FIG. **8** which displays only the ith M-point transform where i=1, . . . ,N. The input of the ith transform is the ith subset of J_i modulated symbols, and the output is the ith frame of M multicoded SS symbols. In FIG. **8**, the ith M-point transform is the randomizing transform **(801)** similar to the randomizing transform **(502)** in FIG. **5** with the set of preset values given as: $a_{1,i}$, $a_{2,i}$, . . . , $a_{M,i}$. In this case, the kth preset value $a_{k,i}$ multiplies the kth subset of J_k modulated symbols to generate the kth multicoded SS symbol.

The ith M-point transform **(801)** in FIG. **8** can further include a second M-point transform **(902)** as described in FIG. **9**.

The first M-point transform **(901)** is the ith randomizing transform with an input of the ith subset of J_i modulated symbols, and an output of the ith frame of M transformed symbols.

The second M-point transform **(902)** is the ith second M-point transform with an input of the ith frame of transformed symbols, and an output of the ith frame of M multicoded SS symbols.

Description of the Transmitter for MCSS Type III

FIG. **10** illustrates a block diagram of the transmitter for MCSS Type III with an input of a stream of data symbols and an output of a stream of multicoded SS symbols. FIG. **10** is described as follows:

The first block is a channel encoder/modulator **(1001)** with an input of a stream of data symbols and an output of a stream of modulated symbols. The function of the channel encoder/modulator is similar to the channel encoder/modulator for MCSS types I and II **(103)** and **(603)** respectively except its operation is serial. Such a representation is commonly used in textbooks to implicitly imply that the data rate of the output stream of modulated symbols could be different from the input stream of data symbols. In other words, the channel encoder/modulator can add redundancy to the input stream of data symbols to protect it against channel distortion and noise. The type of redundancy varies depending on the type of encoding used. In block encoding, the redundancy depends only on the current

block of data. In convolutional encoding, it depends on the current block and parts of the previous block of data. In both types of encoding trellis coding can be used which modulates the modulated symbols output from the encoder.

Even though FIG. **10** does not contain an interleaver, it is possible to include one either before the channel encoder/modulator or after.

The second block is a spreader type III (**1002**) with an input of a stream of modulated symbols and an output of a stream of multicoded SS symbols. The spreader type III is further explained in FIGS. **11**–**13**.

The third block is a ramper (**1003**) with an input of multicoded SS symbols and an output of a ramped multicoded SS symbols. The ramper is further explained in FIG. **14**.

The spreader type II (**1002**) in FIG. **10** is describe further in FIG. **11** as two blocks with an input of a stream of modulated symbols, generated by the channel encoder/modulator (**1001**) in FIG. **10**, and an output of a stream of multicoded SS symbols.

The first block is a randomizer (**1101**) with an input of a stream of modulated symbols and an output of a randomized modulated symbols. The randomizer is described further in FIG. **12**.

The second block is a computing means (**1102**) with an input of the stream of randomized modulated symbols and an output of a stream of multicoded SS symbols. The computing means is described further in FIG. **13**.

In FIG. **12** the randomizer (**1101**) from FIG. **11** is described further as two parts.

The first part is a chip-by-chip multiplier (**1201**) with two inputs and one output. The first input is the stream of modulated symbols and the second input is a stream of preset values output from a randomizing lookup table (**1202**). The output is the product between the two inputs obtained chip-by-chip, i.e. the kth randomized modulated symbols is obtained by multiplying the kth modulated symbol with the kth preset value a_k.

The second part is the randomizing lookup table (**1202**) which is the source of a stream of preset values: . . . ,a_k,a_{k+1}, . . . As mentioned before, the randomizing sequence is only pseudo-randomizing the modulated symbols.

In FIG. **13** the computing means (**1102**) from FIG. **11** is described further as a filter which performs the invertible randomized spreading of the stream of modulated symbols.

FIG. **14** illustrates the ramper (**1003**) in FIG. **10** as a mixer with two inputs and one output. The first input is the stream of multicoded SS symbols, the second input is a linearly ramping carrier frequency $e^{j2\pi f_o t^2}$ which ramps the multicoded SS stream over the time 't' thereby generating a stream of ramped multicoded SS symbols where $j=\sqrt{-1}$ and f_o is a constant.

Description of the Receiver for MCSS Type I

FIG. **15** illustrates a block diagram of the receiver for MCSS type I & II with an input of PM multicoded SS symbols, every PMT_C seconds and an output of VB estimated data symbols, every VBT seconds. FIG. **15** is described as follows:

The first block in FIG. **15** is a serial-to-parallel converter (**1501**) with an input of M multicoded SS symbols and an output of one frame of M multicoded SS symbols every MT_C seconds.

The second block is a 2 Dimensional (2D) shift register (**1502**) with an input of one frame of M multicoded SS symbols each (input by shifting the frame from left to right P times) and an output of P frames of M multicoded SS symbols each, every PMT_C seconds.

The third block is a despreader type I (**1503**) with an input of P frames of M multicoded SS symbols each and an output of P frames of J despread symbols each every PMT_C seconds. The despreader type I is further explained below.

The fourth block is a channel decoder/demodulator (**1504**) with an input of P frames of J despread symbols each and an output of V frames of B estimated data symbols each, every VBT seconds. The channel decoder/demodulator performs two functions: (1) to map the despread symbols into protected data symbols and (2) either to detect errors, or to correct errors, or both. Sometimes, the two functions can be performed simultaneously. In this case, the channel decoder/demodulator performs soft-decision decoding, otherwise, it performs hard-decision decoding. By performing the two function, the channel encoder/demodulator accepts the despread symbols and generates estimated data symbols

The fifth block is a 2 Dimensional (2D) shift register (**1505**) with an input of V frames of B estimated data symbols each, and an output of V frames of B estimated data symbols (output by shifting the V frames from left to right) every VBT seconds. If the 2D shift register (**102**) is operated with B>1, then it might act as an interleaver. In this case, the receiver requires a de-interleaver which is accomplished using the 2D shift register (**1505**).

The sixth block is a parallel-to-serial converter (**1506**) with an input of one frame of B estimated data symbols and an output of B estimated data symbols, every VBT seconds.

The despreader type I (**1504**) in FIG. **15** is described further in FIG. **16** with an input of P frames of M multicoded SS symbols each from the received sequence of multicoded SS symbols, and an output of P frames of J despread symbols each. FIG. **16** is described as follows:

The first block in FIG. **16** is a set of P parallel-to-serial converters (**1601**) with an input of one frame of M multicoded SS symbols per converter, and an output of M multicoded SS symbols per converter.

The second block is a set of N computing means (**1602**) each having the same input of M multicoded SS symbols and an output of one computed value per computing means.

The third block is a detector (**1603**) with an input of N computed values and an output of J despread symbols per detector. When the data symbols are digital, the detector can make either hard decisions or soft decisions. When the data symbols are analog, L_i is necessarily equal to 1 for i=1, . . . ,N and the detector is not required.

The set of N computing means (**1602**) in FIG. **16** is described further in FIG. **17** which displays only the ith computing mean where i=1, . . . ,N. The ith computing mean has as an input the M multicoded SS symbols, and as an output the ith computed value. FIG. **17** is described as follows.

The first block in FIG. **17** is a set of L_i partial correlators (**1701**). The nth partial correlator has two inputs where n=1,2, . . . ,L_i. The first input consists of the M multicoded SS symbols and the second input consists of the nth spread spectrum code of length M chips out

of the ith source of L_i spread spectrum codes. The output of the nth partial correlator is the nth partially correlated value obtained by correlating parts of the first input with the corresponding parts of the second input.

The second block is the ith source (**1702**) of L_i spread spectrum codes with an output of L_i spread spectrum codes of length M chips each.

The third block is the ith sub-detector (**1703**) with an input of L_i partially correlated values and an output of the ith computed value. The ith sub-detector has two tasks. First using the L_i partially correlated values it has to obtain the full correlation between the M multicoded SS symbols and each one of the L_i spread spectrum codes of length M chips obtained from the ith source (**1702**). Then, it has to select the spread spectrum code corresponding to the largest correlation. Such a detected spread spectrum code together with the corresponding full correlation value form the ith computed value.

The detector (**1703**) in FIG. **16** takes all the computed values from each one of the N computing means and outputs J despread symbols. Based on the function of each sub-detector, one can say that the detector (**1603**) has two tasks at hand. First, it has to map each detected spread spectrum code into a first set of despread symbols, then it has to map each full correlation value into a second set of despread symbols. In other words, the first set of despread symbols correspond to spread spectrum codes that form a subset of the spread spectrum codes corresponding to the second set of despread symbols.

It is also possible to have several layers of sub-detectors completing different levels of partial correlations and ending with N spread spectrum codes corresponding to the largest full correlation values per computing means. In this case, the tasks of the detector are first to map each detected spread spectrum code (obtained through the several layers of sub-detection) into sets of despread symbols, then to map each full correlation value into a final set of despread symbols.

Description of the Receiver for MCSS Type II

FIG. **15** illustrates a block diagram of the receiver for MCSS Type II with an input of PM multicoded SS symbols every PMT_C seconds and an output of VB estimated data symbols every VBT seconds. FIG. **15** illustrates also the block diagram of the receiver for MCSS Type I and has been described above.

The despreader type II (**1504**) in FIG. **15** is described further in FIG. **18** with an input of P frames of M multicoded SS symbols each, and an output of P frames of J despread symbols each. FIG. **18** is described as follows:

The first block in FIG. **18** is a set of P M-point transforms (**1801**) with an input of one frame of M multicoded SS symbols per transformer, and an output of M transformed symbols per transformer.

The second block is a set of P detectors (**1802**) with an input of M transformed symbols per detector, and an output of J despread symbols per detector. Once again the detector can either make soft decisions or hard decisions.

Description of the Receiver for MCSS Type III

FIG. **19** illustrates a block diagram of the receiver for MCSS Type III with an input of a stream of ramped multicoded SS symbols and an output of a stream of estimated data symbols. FIG. **19** is described as follows:

The first block in FIG. **19** is a de-ramper (**1901**) with an input of the stream of ramped multicoded SS symbols and an output of an estimated stream of multicoded SS symbols. The de-ramper is further described in FIG. **20**.

The second block is a de-spreader Type III (**1902**) with an input of the estimated stream of multicoded SS symbols and an output of a stream of detected symbols. The de-spreader type II is further explained in FIG. **21–23**.

The third block is a channel decoder/demodulator (**1903**) with the input consisting of the stream of detected symbols, and an output of a stream of estimated data symbols. It is clear from FIG. **19** that no de-interleaver is included in the receiver. As mentioned above, if an interleaver is added to the transmitter in FIG. **10**, then FIG. **19** requires a de-interleaver.

FIG. **20** illustrates the deramper (**1901**) in FIG. **19** as a mixer with two inputs and one output. The first input is the ramped multicoded SS symbols and the second input is a linearly ramping carrier frequency which deramps the ramped multicoded SS stream thereby generating an estimated stream of multicoded SS symbols.

The despreader type III (**1902**) in FIG. **19** is described further in FIG. **21** as three blocks.

The first block is a computing means (**2101**) with an input of an estimated stream of multicoded SS symbols and an output of a stream of randomized despread symbols. FIG. **22** describes the computing means (**2101**) in FIG. **21** as a filter (**2201**) which performs the despreading process.

The second block is a de-randomizer (**2102**) with an input of a stream of randomized despread symbols and an output of a stream of despread symbols. The de-randomizer (**2102**) is described further in FIG. **23**.

The third block is a detector (**2103**) with an input of a stream of despread symbols and an output of a stream of detected symbols. When the detector is a hard-decision detector it makes a decision on the despread symbols such that the detected values takes a finite number of values out of a predetermined alphabet of finite size. When the detector is a soft-decision detector the detected symbols are the same as the despread symbols.

The de-randomizer (**2102**) is described further in FIG. **23** as two parts.

The first part is a chip-by-chip multiplier (**2301**) with two inputs and an output. The first input is a stream of randomized despread data symbols and the second input is a stream of preset values output from a de-randomizing lookup table (**2302**). The output is the chip-by-chip product between the two inputs, i.e. the kth despread symbol is obtained as the product between the kth randomized despread symbol and the kth preset value b_k.

The second part is a de-randomizing lookup table (**2302**) which outputs a stream of preset values: $\ldots, b_k, b_{k+1}, \ldots$

PREFERRED EMBODIMENTS OF THE INVENTION

From the above description of the invention, it is clear that the contribution of the invention is primarily in the spreader in the transmitter and in the despreader in the receiver for each one of the three type of MCSS introduced in the patent. The secondary contribution of the patent resides in the channel encoder/modulator and in the extra components that can be used in both the transmitter and in the receiver for each three types such as: the ramping and de-ramping of the signal and diversity techniques. For these reasons, we have

separated the preferred embodiments of the invention into three parts. Each part corresponds to the spreader and the despreader for each one of the three types of MCSS and its extras.

Preferred Embodiments of the Spreader/Despreader for MCSS Type I

In FIG. **1**, the spreader Type I (**104**) performs an invertible randomized spreading of the modulated symbols which carry either digital information or analog information, and in FIG. **15** the despreader Type I (**1503**) performs a reverse operation to the spreader Type I (**104**) within the limits of available precision (i.e. with some level of quantization noise).

In FIG. **1**, the spreader Type I (**104**) performs an invertible randomized spreading of the modulated, and in FIG. **15** the despreader Type I (**1503**) performs a reverse operation to the spreader Type I (**104**) while taking into account the effects of the communications channel such as noise, distortion and interference. The effects of the channel are sometimes unknown to the receiver (e.g. over selective fading channels which cause intersymbol interference). In such cases, the channel has to be estimated using for example a pilot signal known to the receiver as in "MultiCode Direct Sequence Spread Spectrum," by M. Fattouche and H. Zaghloul, U.S. Pat. No. 5,555,268, September 1996.

In FIG. **2**, if $J_k=0$ for any k=1, . . . ,N then the output of the kth computing means is the all zeros spread spectrum codes of length M chips.

In FIG. **2**, if the modulated symbols are M-ary symbols, then a preferred value for L_i is M to the power of J_i. In other words, by choosing one spread spectrum code out of L_i codes, J_i symbols of information are conveyed.

In FIG. **3**, a preferred function for the ith mapper is to choose one spread spectrum code (out of the L_i available codes) based on one part of the ith subset of J_i modulated symbols while the second part of the subset is used to choose the symbol that multiplies the chosen spread spectrum code. In other words, assuming that the kth spread spectrum code S_k is chosen by the ith mapper (**301**) (out of the L_i available codes) based on the first part of the ith subset of J_i modulated symbols and that the symbol ζ is chosen to multiply S_k based on the second part of the ith subset of J_i modulated symbols, then the ith spread spectrum symbol out of the ith mapper (**301**) is $S^k\zeta$. This is equivalent to spreading ζ over S_k.

In FIG. **3**, ζ can be chosen as a DBPSK symbol, a DQPSK symbol, a DMPSK symbol, a QAM symbol, a FSK symbol, a CPM symbol, an ASK symbol, etc.

In FIG. **3**, the L_i spread spectrum codes, out of the ith source (**302**) of L_i available spread spectrum codes, correspond to Walsh codes. Each Walsh code in FIG. **3** is generated in FIG. **4** as the output of an M-point Walsh transform where the input is a preset sequence of length M chips with (M−1) chips taking a zero value while one chip taking a unity value.

In FIG. **3**, the L_i spread spectrum codes, out of the ith source (**302**) of L_i available spread spectrum codes, correspond to randomized Walsh codes. Each Walsh code generated in FIG. **4** as the output of an M-point Walsh transform is randomized in FIG. **5** using a chip-by-chip multiplier where the kth chip of each Walsh code is multiplied by the preset value $a_{k,i}$ output from the ith randomizing lookup table.

In FIG. **5**, them preset values $\{a_{1,i},a_{2,i}, \ldots ,a_{M,i}\}$ are chosen such that their amplitudes: $|a_{1,i}|,|a_{2,i}|, \ldots ,|a_{M,i}|$ are all equal to unity.

In FIG. **3**, a preferred value for L_i is 2 and a preferred value for M is 10 with the two preferred spread spectrum codes out of the ith source (**302**) taking the values:

$$\{c_1,c_2,c_3,c_4,c_5,c_6,c_7,c_8,c_9,c_{10}\}$$

and

$$\{c_1,c_2,c_3,c_4,c_5,-c_6,-c_7,-c_8,-c_9,-c_{10}\} \quad (1)$$

In equation (1), preferred values for the chips '$c_1,c_2,c_3,c_4,c_5,c_6,c_7,c_8,c_9,c_{10}$' are '1,−1,1,1,1,j,−j,j,j,j' which we refer to as the 'Wi-LAN codes Type I'.

Preferred Embodiments of the Spreader/Despreader for MCSS Type II

In FIG. **6**, the spreader Type II (**604**) performs an invertible randomized spreading of the modulated symbols which carry either digital information or analog information, and in FIG. **15** the despreader Type II (**1503**) performs a reverse operation to the spreader Type II (**604**) within the limits of available precision (i.e. with some level of quantization noise).

In FIG. **6**, the spreader Type II (**604**) performs an invertible randomized spreading of the modulated, and in FIG. **15** the despreader Type II (**1503**) performs a reverse operation to the spreader Type II (**604**) while taking into account the effects of the communications channel such as noise, distortion and interference. As mentioned above, the effects of the channel are sometimes unknown to the receiver (e.g. over selective fading channels which cause intersymbol interference). In such cases, the channel has to be estimated using for example a pilot signal known to the receiver as in "MultiCode Direct Sequence Spread Spectrum," by M. Fattouche and H. Zaghloul, U.S. Pat. No. 5,555,268, September 1996.

Two preferred types of pilot signals can be used to estimate the effects of the channel on the information-bearing data symbols:

1. Pilot Frames inserted either before, during or after the Data frames of M multicoded SS symbols; and
2. Pilot Symbols inserted within each data frame of M multicoded SS symbols.

Pilot frames estimate the long term effects of the channel, while pilot symbols estimate the short term effects of the channel.

When channel estimation is used in the receiver as mentioned above, it is possible to use coherent detection with phase modulation, such as BPSK, QPSK and MPSK, after removing the effects of the channel from the phase of the received signal. On the other hand, if the effects of the channel are not removed, differential detection is selected instead with differentially-encoded phase modulation such as DPSK, DQPSK and DMPSK.

Furthermore, when channel estimation is used in the receiver as mentioned above, it is possible to use amplitude modulation together with coherent detection of phase modulation, such as ASK and QAM, after removing the effects of the channel from the phase and the amplitude of the received signal. On the other hand, if the effects of the channel are not removed, differential detection is selected instead with differentially-encoded phase and amplitude modulation such as Differential QAM using the star constellation.

A preferred modulation technique is QAM when the channel is estimated and its effects removed.

Another preferred modulation technique is DMPSK when the effects of the channel are not removed. In this case, a reference symbol is chosen at the beginning of each frame output from the channel modulator/modulator **(603)**.

In FIG. **6**, a preferred channel encoder/modulator **(603)** is a Reed-Solomon channel encoder used for encoding M-ary symbols and for correcting errors caused by the channel at the receiver. If the data symbols are binary, it is preferred to choose to combine several input bits into one symbol prior to encoding. A preferred technique to combine several bits into one symbol is to combine bits that share the same position within a number of consecutive frames. For example, the kth bit in the nth frame can be combined with the kth bit in the (n+1)th frame to form a dibit, where k=1, . . . ,Q.

In FIG. **6**, if the data symbols are M-ary, a preferred value for B is unity when using a Reed-Solomon encoder, i.e. no interleaver is required in this case.

In FIG. **7**, preferred values for $J_1, J_2, \ldots, J_M$ are unity.

In FIG. **8**, preferred values for $\{a_{1,i}, a_{2,i}, \ldots, a_{M,i}\}$ are such that their amplitudes: $|a_{1,i}|, |a_{2,i}|, \ldots, |a_{M,i}|$ are all equal to unity.

In FIG. **9**, preferred ith second M-point transform **(902)** is a Discrete Fourier Transform (DFT).

When $J_1=J_2=\ldots=J_M=1$, $|a_{1,i}|=|a_{2,i}|=\ldots=|a_{M,i}|=1$ and the ith second M-point transform is a DFF, the MCSS transmitter is similar to the one in the issued patent: "Method and Apparatus for Multiple Access between Transceivers in Wireless Communications using OFDM Spread Spectrum," by M. Fattouche and H. Zaghloul, U.S. Pat. No. 5,282,222, Jan. 25, 1994.

The generated spread spectrum codes using

$$J_1=J_2=\ldots=J_M=1,$$

$$|a_{1,i}|=|a_{2,i}|=\ldots=|a_{M,i}|=1,$$

the ith second M-point transform as a DFT, and

the channel encoder as a Reed-Solomon encoder without an interleaver are referred to as the 'Wi-LAN codes Type II'.

Another preferred embodiment of the ith second M-point transform **(902)** is a Circular FIR (CFIR) filter of length M coefficients which performs an M-point circular convolution between each block of M modulated symbols and its own coefficients. In this case, a preferred embodiment of the M-point transform **(1801)** is also a CFIR filter of length M coefficients which performs the inverse operation of the spreading CFIR filter by performing an M-point circular convolution between each block of M multicoded SS symbols and its own coefficients. When the channel is estimated, the despreading CFIR filter can also invert the effects of the channel using either

1. a linear algorithm such as Zero Forcing Equalization (ZFE) and Minimum Mean Square Equalization (MMSE); or
2. a nonlinear algorithm such as Decision Feedback Equalization (DFE) and Maximum Likelihood (ML).

The effect of a nonideal frequency-selective communication channel is to cause the multicodes to loose their orthogonality at the receiver. In the case when ZFE is employed, the CFIR filter acts as a decorrelating filter which decorrelates the M multicoded symbols from one another at the receiver thereby forcing the symbols to be orthogonal.

An advantage of using CFIR filter for spreading and despreading the data symbols is that IF-sampling can be inherently employed in the MCSS receiver without increasing the complexity of the digital portion of the receiver since interpolation and decimation filters can be included in the CFIR filters.

Preferred Embodiments of the Spreader/Despreader for MCSS Type III

In FIG. **10**, the spreader Type III **(1002)** performs an invertible randomized spreading of the stream of modulated symbols which carry either digital information or analog information, and in FIG. **19** the despreader Type I **(1902)** performs a reverse operation to the spreader Type III **(1002)** within the limits of available precision (i.e. with some level of quantization noise).

In FIG. **10**, the spreader Type III **(1002)** performs an invertible randomized spreading of the stream of modulated symbols, and in FIG. **19** the despreader Type III **(1902)** performs a reverse operation to the spreader Type III **(1002)** while taking into account the effects of the communications channel such as noise, distortion and interference. As mentioned above, the effects of the channel are sometimes unknown to the receiver (e.g. over selective fading channels which cause intersymbol interference). In such cases, the channel has to be estimated using for example a pilot signal known to the receiver as in "MultiCode Direct Sequence Spread Spectrum," by M. Fattouche and H. Zaghloul, U.S. Pat. No. 5,555,268 September 1996.

A preferred randomizer **(1101)** in FIG. **11** is a trivial one with no effect on the modulated symbols.

Another preferred randomizer **(1101)** is one where the preset values out of the randomizing lookup table **(1202)**: $\{\ldots, a_{k-1}, a_k, a_{k+1}, \ldots\}$ have amplitudes which are equal to unity.

In FIG. **13**, a preferred filter is a Finite Impulse Response (FIR) filter with the coefficients obtained as the values of a polyphase code.

In FIG. **13**, a preferred filter is an FIR filter with the coefficients obtained as approximations to the values of a polyphase code.

In FIG. **13**, a preferred filter is an FIR filter with the following **16** coefficients:

$$\{1,1,1,1,1,j,-1,-j,1,-1,1,-1,1,-j,-1,j\}$$

forming its impulse response where $j=\sqrt{-1}$. The 16 coefficients correspond to the following polyphase code:

$$\{e^{j0\theta(0)},e^{j1\theta(0)},e^{j2\theta(0)},e^{j3\theta(0)},e^{j0\theta(1)},e^{j1\theta(1)},e^{j2\theta(1)},e^{j3\theta(1)},e^{j0\theta(2)},e^{j\theta(2)},\\ e^{j2\theta(2)},e^{j3\theta(2)},e^{0\theta(3)},e^{j\theta(3)},e^{j2\theta(3)},e^{j3\theta(3)}\}$$

where $\theta(0)=0$, $\theta(1)=2\pi/4$, $\theta(2)=4\pi/4$, $\theta(3)=6\pi/4$, and $j=\sqrt{-1}$.

In FIG. **13**, another preferred filter is an FIR filter with 64 coefficients corresponding to the following polyphase code:

$$\{e^{j0\theta(0)},e^{j1\theta(0)},e^{j2\theta(0)},e^{j3\theta(0)},e^{j4\theta(0)},e^{j5\theta(0)},e^{j6\theta(0)},e^{j7\theta(0)},e^{j0\theta(1)},e^{j1\theta(1)},\\ e^{j2\theta(1)},e^{j3\theta(1)},e^{j4\theta(1)},e^{j5\theta(1)},e^{j6\theta(1)},$$

$$e^{j7\theta(1)},e^{j0\theta(2)},e^{j1\theta(2)},e^{j2\theta(2)},e^{j3\theta(2)},e^{j4\theta(2)},e^{j5\theta(2)},e^{j6\theta(2)},e^{j7\theta(2)},e^{j0\theta(3)},\\ e^{j1\theta(3)},e^{j2\theta(3)},e^{j3\theta(3)},e^{j4\theta(3)},e^{j5\theta(3)},e^{j6\theta(3)},$$

$$e^{j7\theta(3)},e^{j0\theta(4)},e^{j1\theta(4)},e^{j2\theta(4)},e^{j3\theta(4)},e^{j4\theta(4)},e^{j5\theta(4)},e^{j6\theta(4)},e^{j7\theta(4)},e^{j0\theta(5)},e^{j1\theta(5)},e^{j2\theta(5)},e^{j3\theta(5)},e^{j4\theta(5)},e^{j5\theta(5)},e^{j6\theta(5)},$$

$$e^{j7\theta(5)},e^{j0\theta(6)},e^{j1\theta(6)},e^{j2\theta(6)},e^{j3\theta(6)},e^{j4\theta(6)},e^{j5\theta(6)},e^{j6\theta(6)},$$

$$e^{j7\theta(6)},e^{j0\theta(7)},e^{j1\theta(7)},e^{j2\theta(7)},e^{j3\theta(7)},e^{j4\theta(7)}e^{j5\theta(7)},e^{j6\theta(7)},e^{j7\theta(7)}\}$$

where $\theta(0)=0$, $\theta(1)=2\pi/8$, $\theta(2)=4\pi/8$, $\theta(3)=6\pi/8$, $\theta(4)=8\pi/8$, $\theta(5)=10\pi/8$, $\theta(6)=12\pi/8$, $\theta(7)=14\pi/8$, and $j=\sqrt{-1}$.

In general, a preferred filter in FIG. **13** with M coefficients corresponding to a polyphase code can be obtained as the concatenation of the rows of an $\sqrt{M}\times\sqrt{M}$ matrix (assuming $\sqrt{M}$ is an integer) with the coefficient in the ith row and kth column equal to $e^{j(i-1)\theta(k-1)}$ where $\theta(k)=2\pi k/\sqrt{M}$, and $j=\sqrt{-1}$.

Another preferred filter in FIG. **13** with M coefficients corresponding to a binary approximation of a polyphase code can be obtained as the concatenation of the rows of an $\sqrt{M}\times\sqrt{M}$ matrix with the coefficient in the ith row and kth column determined as follows:

when $(i-1)\theta(k-1)$ is an integer number of $\pi/2$, the coefficient is equal to $e^{j(i-1)\theta(k-1)}$ where $\theta(k)=2\pi k/\sqrt{M}$, otherwise

when $(i-1)\theta(k-1)$ is not an integer number of $\pi/2$, the coefficient is equal to $e^{jn\pi/2}$ where n is an integer number which minimizes the value: $(n\pi/2-(i-1)\theta(k-1))^2$.

We refer to the spread spectrum code corresponding to the coefficients of a filter representing a binary approximation of a polyphase code as discussed above as the 'Wi-LAN code Type III'.

For example when M=64, the above procedure produces the following filter coefficients:

{1,1,1,1,1,1,1,1,1,1,j,j,−1,−1,−j,−j,1,j,−1,−j,1,j,−1,−j,1,j,−j,1,−1,−j, j,−1,1,−1,1,−1,1,−1,1,−1,1,−1,j,−j,−1,1,−j,j,1,−j,−1,j,1,−j,−1,j,1,−j,−j,−1,−1,j,j,1}

A preferred filter in FIG. **21** performs a reverse operation to the filter **(1301)** in FIG. **13**.

Another preferred filter in FIG. **21** performs a matching filtering operation to the filter **(1301)** in FIG. **13**.

A preferred de-randomizer **(2102)** in FIG. **21** is one where the preset values out of the de-randomizing lookup table **(2302)**: $\{\ldots,b_{k-1},b_k,b_{k+1},\ldots\}$ performs a reverse operation to the randomizer **(1101)** in FIG. **11**.

Another preferred de-randomizer **(2102)** in FIG. **21** is one where the preset values out of the de-randomizing lookup table **(2302)**: $\{\ldots,b_{k-1},b_k,b_{k+1},\ldots\}$ are equal to the reciprocal of the preset values out of the randomizing lookup table **(1202)** in FIG. **12**, i.e. $b_k=1/a_k$ for all values of k.

A preferred diversity technique for MCSS Type III is shown in FIG. **24** where we have L branches with one de-ramper **(2401)** per branch. Each de-ramper linearly de-ramps the received signal using a linearly deramping carrier frequency of fixed slope and unique intercept. Each intercept corresponds to a unique time of arrival of the different multipath components. The outputs of the L de-rampers are then combined in the combiner **(2402)** using any appropriate combining technique such as: co-phasing combining, maximum ratio combining, selection combining, equal gain combining, etc. The output of the combiner is then despread using the de-spreader **(2403)** and input into the channel decoder/demodulator **(2404)** to generate the estimated data symbols.

A preferred value for f_o in FIG. **14** is $1/(2\tau MT_C)$ where τ is the relative delay between the first arriving radio signal and the second arriving radio signal at the receiver, M is the number of coefficients in the spreading filter **(1301)** in FIG. **13** and T_C is the duration of one chip (or equivalently it is the unit delay in the spreading filter **(1301)**). In other words, the symbol rate at both the input and the output of the spreading filter **(1301)** is $1/T_C$.

The entire disclosure of U.S. Pat. No. 5,282,222 issued Jan. 25, 1994, and U.S. Pat. No. 5,555,268 issued Sep. 10, 1996, are hereby incorporated by reference in their entirety in this patent document.

A person skilled in the art could make immaterial modifications to the invention described in this patent document without departing from the essence of the invention that is intended to be covered by the scope of the claims that follow.

We claim:

1. A transceiver for transmitting a first stream of data symbols, the transceiver comprising:

a first converter for converting the first stream of data symbols into plural sets of B data symbols each;

a channel encoder/modulator for encoding the plural sets of B data symbols into plural sets of J modulated symbols;

a spreader for spreading the plural sets of J modulated symbols into plural sets of N spread spectrum symbols of length M chips each;

M combiners for combining each set of the plural sets of N spread spectrum symbols into M multicoded SS symbols; and

a second converter for converting the plural sets of M multicoded SS symbols into a first stream of multicoded SS symbols for transmission.

2. The transceiver if claim **1** in which the spreader includes:

a third converter for converting each one of the plural sets of J modulated symbols into N subsets of modulated symbols; and

a set of N computing means for operating on each one of the N subsets of modulated symbols to produce the N spread spectrum symbols whereby an ith set of computing means operates on an ith subset of modulated symbols to produce an ith spread spectrum symbol.

3. The transceiver of claim **2** in which the ith computing means includes:

a source of available spread spectrum codes; and

a modulator to choose for each ith subset of modulated symbols one spread spectrum code from the source of available spread spectrum codes to become the spread spectrum code representing the ith subset of modulated symbols, thereby spreading each subset of modulated symbols over a separate spread spectrum code.

4. The transceiver of claim **3** in which the spread spectrum codes are generated by operation of a non-trivial transform on a sequence of input signals.

5. The transceiver of claim **4** in which the non-trivial transform consists of either a Walsh transform or a Fourier transform followed by a randomizing transform.

6. The transceiver of claim **3** further including:

means for receiving a sequence of multicoded SS symbols, the multicoded SS symbols having been generated by spreading a second stream of data symbols;

a third converter for converting the received stream of multicoded SS symbols into plural sets of M multicoded SS symbols each;

a despreader for despreading plural sets of M multicoded SS symbols to produce plural sets of J despread symbols;

a channel decoder/demodulator for decoding plural sets of J despread symbols into plural sets of B estimated data symbols of the second stream of data symbols; and

a fourth converter for converting the plural sets of the B estimated data symbols into a stream of estimated data symbols of the second stream of data symbols.

7. The transceiver of claim **6** in which the despreader includes:

a set of N computing means to operate on the set of M multicoded SS symbols, from the received sequence of multicoded SS symbols, to generate a set of N computed values; and

a detector for operating on the set of N computed values to generate a set of J despread symbols.

8. The transceiver of claim **7** in which the ith computing means includes:

a set of partial correlators for partially correlating the set of M multicoded SS symbol with corresponding parts of each spread spectrum code from the ith source of available spread spectrum codes to generate partially correlated values; and

a sub-detector for operating on the partially correlated values to produce the ith computed value.

9. The transceiver of claim **1** in which the spreader is based on Wi-LAN codes Type I.

10. A transceiver for transmitting a first stream of data symbols, the transceiver comprising:

a first converter for converting the first stream of data symbols into plural sets of B data symbols each;

a channel encoder/modulator for encoding plural sets of B data symbols into plural sets of J modulated symbols;

a spreader for spreading plural sets of J modulated symbols into plural sets of M multicoded SS symbols; and

a second converter for converting the plural sets of M multicoded SS symbols into a first stream of multicoded SS symbols for transmission.

11. The transceiver of claim **10** in which the spreader includes:

a third converter for converting each one of the plural sets of J modulated symbols into M subsets of modulated symbols; and

a transformer for operating on the M subsets of modulated symbols to generate M multicoded SS symbols as output, the M multicoded SS symbols corresponding to spreading each subset of modulated symbol over a separate spread spectrum symbol and combining the M spread spectrum symbols.

12. The transceiver of claim **11** in which the transformer effectively applies a first transform corresponding to a randomizing transform of the M data symbols.

13. The transceiver of claim **12** in which the first transform is followed by a second transform corresponding to a Fourier transform.

14. The transceiver of claim **10** in which the channel encoder/modulator includes a Reed-Solomon encoder.

15. The transceiver of claim **10** in which the J modulated symbols contain a number of pilot symbols.

16. The transceiver of claim **10** in which plural sets of M multicoded SS symbols correspond to plural sets of M pilot symbols.

17. The transceiver of claim **12** in which the first transform is followed by a second transform corresponding to a circular finite impulse response filter.

18. The transceiver of claim **11** further including:

means for receiving a sequence of multicoded SS symbols, the multicoded SS symbols having been generated by spreading a second stream of data symbols;

a third converter for converting the received stream of multicoded SS symbols into plural sets of M multicoded SS symbols each;

a despreader for despreading plural sets of M multicoded SS symbols to produce plural sets of J despread symbols;

a channel decoder/demodulator for decoding plural sets of J despread symbols into plural sets of B estimated data symbols of the second stream of data symbols; and

a fourth converter for converting the plural sets of the B estimated data symbols into a stream of estimated data symbols of the second stream of data symbols.

19. The transceiver of claim **10** in which the spreader is based on Wi-LAN codes Type II.

20. A transceiver for transmitting a first stream of data symbols, the transceiver comprising:

a channel encoder/modulator for encoding the first stream of data symbols into a modulated stream; and

a spreader for spreading the modulated stream into a multicoded SS stream corresponding to an invertible randomized spreading of the modulated stream.

21. The transceiver of claim **20** further including means to ramp the multicoded SS stream using a linearly ramping carrier frequency, thereby generating a stream of ramped multicoded SS symbols.

22. The transceiver of claim **20** in which the spreader comprises:

a randomizer for randomizing the modulated stream into a randomized modulated stream; and

a filter for spreading the randomized modulated stream into a multicoded SS stream.

23. The transceiver of claim **22** in which the filter has a finite impulse response and the coefficients of the impulse response are chosen from a set of spread spectrum codes.

24. The transceiver of claim **23** in which the set of spread spectrum codes is the class of polyphase codes.

25. The transceiver of claim **23** in which the set of spread spectrum codes is the class of codes that represent a binary approximation of the polyphase codes.

26. The transceiver of claim **1**, or claim **10**, or claim **20** in which the spreader is wideband.

27. The transceiver of claim **20** further including:

means for receiving a stream of multicoded SS symbols, the multicoded SS symbols having been generated by encoding and invertible randomized spreading of a second stream of data symbols;

a despreader for despreading the received stream of multicoded SS symbols into a detected stream; and

a channel decoder/demodulator for decoding the detected stream to produce an estimate of the second stream of data symbols.

28. The transceiver of claim **20** in which the spreader is based on Wi-LAN codes Type III.

29. A method of exchanging data streams between a plurality of transceivers, the method comprising the steps of:

converting a first stream of data symbols into plural sets of B data symbols each;

channel encoding plural sets of B data symbols into plural sets of J modulated symbols;

spreading plural sets of J modulated symbols into plural sets of N spread spectrum symbols of length M chips each;

combining each set of the plural sets of the N spread spectrum symbols into M multicoded SS symbols;

converting the plural sets of M multicoded SS symbols into a first stream of multicoded SS symbols for transmission; and

transmitting the multicoded SS symbols from a first transceiver at a time when no other of the plurality of transceivers is transmitting.

30. The method of claim **29** in which spreading of plural sets of J modulated symbols into plural sets of N spread spectrum symbols includes the step of: converting each one of the plural sets of J data symbols into N subsets of data symbols.

31. The method of claim **30** in which spreading of plural sets of J modulated symbols into plural sets of N spread spectrum symbols further includes: choosing for each ith subset of modulated symbols one spread spectrum code from a number of available spread spectrum codes to become the spread spectrum symbol representing the ith subset of modulated symbols, thereby spreading each subset of modulated symbols over a separate spread spectrum code.

32. The method of claim **31** further including the steps of:

receiving, at a transceiver distinct from the first transceiver, the sequence of multicoded SS symbols;

converting the received stream of multicoded SS symbols into plural sets of M multicoded SS symbols each;

despreading plural sets of M multicoded SS symbols to produce plural sets of J despread symbols;

decoding plural sets of J despread symbols into plural sets of B estimated data symbols of the first stream of data symbols; and

converting the plural sets of the B estimated data symbols into a stream of estimated data symbols of the first stream of data symbols.

33. The method of claim **32** in which despreading the received sequence of multicoded SS symbols includes the steps of:

partially correlating each set of M multicoded SS symbols from the received sequence of multicoded SS symbols with corresponding parts of each spread spectrum code from the set of available spread spectrum codes;

operating on the partially correlated values through the use of a set of N sub-detectors to produce a set of N computed values; and

operating on the set of N computed values through the use of a detector to generate a set of J despread symbols.

34. The method of claim **29** in which spreading of plural sets of J modulated symbols into plural sets of N spread spectrum symbols is based on a filter with coefficients equal to Wi-LAN codes Type I.

35. A method of exchanging data streams between a plurality of transceivers, the method comprising the steps of:

converting a first stream of data symbols into plural sets of B data symbols each;

channel encoding plural sets of B data symbols into plural sets of J modulated symbols;

spreading plural sets of J modulated symbols into plural sets of M multicoded SS symbols;

converting the plural sets of M multicoded SS symbols into a first stream of multicoded SS symbols for transmission; and

transmitting the multicoded SS symbols from a first transceiver at a time when no other of the plurality of transceivers is transmitting.

36. The method of claim **35** in which spreading of plural sets of J modulated symbols into plural sets of M multicoded SS symbols further includes:

converting each one of the plural sets of J modulated symbols into M subsets of modulated symbols; and

transforming, by way of a transform, the M subsets of modulated symbols to generate M multicoded SS symbols as output, the M multicoded SS symbols corresponding to spreading each subset of modulated symbol over a separate spread spectrum symbol and combining the M spread spectrum symbols.

37. The method of claim **36** in which transforming the M subsets of modulated symbols includes applying to the M subsets of modulated symbols a randomizing transform and a Fourier transform.

38. The method of claim **36** in which transforming the M subsets of modulated symbols includes applying to the M subsets of modulated symbols a randomizing transform and a circular convolution.

39. The method of claim **36** further including the steps of:

receiving, at a transceiver distinct from the first transceiver, the sequence of multicoded SS symbols;

converting the received stream of multicoded SS symbols into plural sets of M multicoded SS symbols each;

despreading plural sets of M multicoded SS symbols to produce plural sets of J despread symbols;

decoding plural sets of J despread symbols into plural sets of B estimated data symbols of the first stream of data symbols; and

converting the plural sets of the B estimated data symbols into a stream of estimated data symbols of the first stream of data symbols .

40. The method of claim **35** in which spreading of plural sets of J modulated symbols into plural sets of N spread spectrum symbols is based on Wi-LAN codes Type II.

41. A method of exchanging data streams between a plurality of transceivers, the method comprising the steps of:

channel encoding a first stream of data symbols into a stream of modulated symbols; and

spreading the stream of modulated symbols to produce a multicoded SS stream corresponding to an invertible randomized spreading of the first modulated stream.

42. The method of claim **41** further including ramping the multicoded SS stream using a linearly ramping carrier frequency, thereby generating a stream of ramped multicoded SS symbols.

43. The method of claim **42** in which spreading the stream of modulated symbols to produce a multicoded SS stream comprises:

randomizing the modulated symbols, through the use of a randomizer to generate a stream of randomized modulated symbols; and

filtering the randomized modulated symbols, through the use of a filter to generate a stream of multicoded SS symbols.

44. The method of claim **29**, or claim **35**, or claim **41** in which spreading is wideband.

45. The method of claim **41** further including the steps of:

receiving, at a transceiver distinct from the first transceiver, the stream of multicoded SS symbols;

despreading the received stream of multicoded SS symbols to produce a detected stream; and

decoding the detected stream to produce an estimate of the first stream of data symbols.

46. The method of claim **42** in which spreading the stream of modulated symbols to produce a multicoded SS stream is based on a filter with coefficients equal to Wi-LAN codes Type III.

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,320,897 B1 Page 1 of 1
DATED : November 20, 2001
INVENTOR(S) : M.T. Fattouche et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page,
Item [75], Inventors, "**Michel T. Fattouche; Hatim Zaghloul; Paul R. Milligan; David L. Snell,** all of Calgary (CA)" should read -- **Michel T. Fattouche; Hatim Zaghloul;** both of Calgary (CA) --

Item [56], **References Cited**, OTHER PUBLICATIONS, insert in appropriate order the following:

-- Bingham, J.A.C., "Multicarrier Modulation for Data Transmission: An Idea Whose Time Has Come", *IEEE Communications Magazine*, pp. 5-15, May 1990.
Spracklen, C.T. and C. Smythe, "The Application of Code Division Multiplexing Techniques to Local Area Networks," pp. 767-770, May 1987. --

Signed and Sealed this

Thirteenth Day of August, 2002

Attest:

JAMES E. ROGAN

Attesting Officer *Director of the United States Patent and Trademark Office*